PENTEK®
Setting the Standard for Digital Signal Processing

Software Defined Radio Handbook
10th Edition

Sampling

Principles of SDR

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by

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Preface

SDR (Software-Defined Radio) has revolutionized electronic systems for a
variety of applications including communications, data acquisition and signal processing.

This handbook shows how DDCs (Digital Downconverters) and DUCs (Digital Upconverters),
the fundamental building blocks of SDR, can replace legacy analog receiver and transmitter designs while
offering significant benefits in performance, density and cost.

In order to fully appreciate the benefits of SDR, conventional analog receiver and transmitter
systems will be compared to their digital counterparts, highlighting similarities and differences.

The inner workings of the SDR will be explored with an in-depth description of the internal
structure and the devices used. Finally, some actual board- and system-level implementations and available
off-the-shelf SDR products and applications based on such products will be presented.

For more information on complementary subjects, the reader is referred to these Pentek Handbooks:
Putting FPGAs to Work in Software Radio Systems
Critical Techniques for High-Speed A/D Converters in Real-Time Systems
High-Speed Switched Serial Fabrics Improve System Design
High-Speed, Real-Time Recording Systems
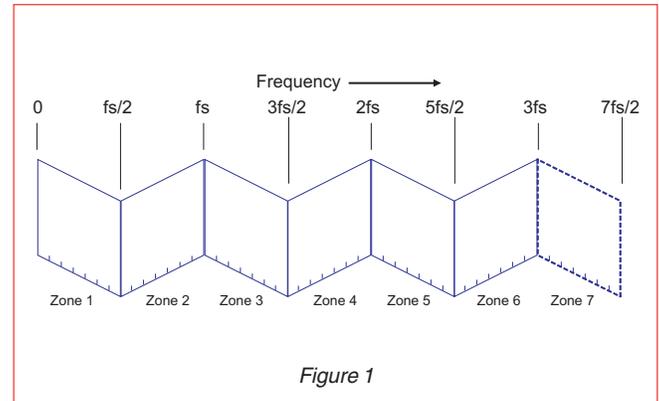
Sampling

Nyquist's Theorem and Sampling

Before we look at SDR and its various implementations in embedded systems, we'll review a theorem fundamental to sampled data systems such as those encountered in Software-Defined Radios.

Nyquist's Theorem:

"Any signal can be represented by discrete samples if the sampling frequency is at least twice the bandwidth of the signal."

Notice that we highlighted the word bandwidth rather than frequency. In what follows, we'll attempt to show the implications of this theorem and the correct interpretation of sampling frequency, also known as sampling rate.

A Simple Technique to Visualize Sampling
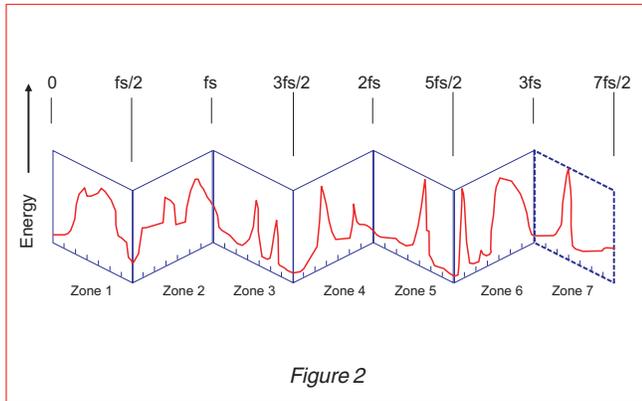

Figure 1

To visualize what happens in sampling, imagine that you are using transparent "fan-fold" computer paper. Use the horizontal edge of the paper as the frequency axis and scale it so that the paper folds line up with integer multiples of one-half of the sampling frequency f_s. Each sheet of paper now represent what we will call a "Nyquist Zone", as shown in Figure 1.
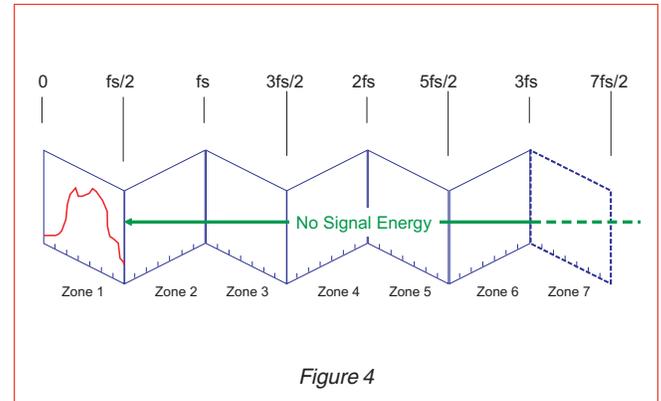
Sampling

Sampling Basics

Figure 2

Use the vertical axis of the fan-fold paper for signal energy and plot the frequency spectrum of the signal to be sampled, as shown in Figure 2. To see the effects of sampling, collapse the transparent fan-fold paper into a stack.

Figure 3
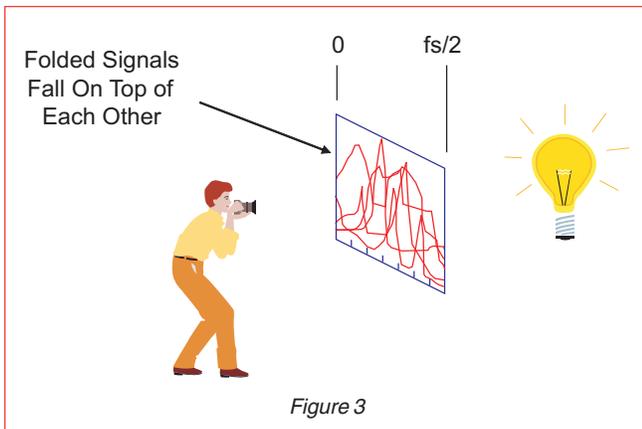
The resulting spectrum can be seen by holding the transparent stack up to a light and looking through it. You can see that signals on all of the sheets or zones are "folded" or "aliased" on top of each other — and they can no longer be separated.

Once this folding or aliasing occurs during sampling, the resulting sampled data is corrupted and can never be recovered. The term "aliasing" is appropriate because after sampling, a signal from one of the higher zones now appears to be at a different frequency.

Baseband Sampling

Figure 4

A baseband signal has frequency components that start at $f = 0$ and extend up to some maximum frequency.

To prevent data destruction when sampling a baseband signal, make sure that all the signal energy falls ONLY in the 1st Nyquist band, as shown in Figure 4.

There are two ways to do this:
1. Insert a lowpass filter to eliminate all signals above $f_s/2$, or
2. Increase the sampling frequency so all signals present fall below $f_s/2$.

Note that $f_s/2$ is also known as the "folding frequency".

Sampling Bandpass Signals

Let's consider bandpass signals like the IF frequency of a communications receiver that might have a 70 MHz center frequency and 10 MHz bandwidth. In this case, the IF signal contains signal energery from 65 to 75 MHz.

If we follow the baseband sampling rules above, we must sample this signal at twice the highest signal frequency, meaning a sample rate of at least 150 MHz.

However, by taking advantage of a technique called "undersampling", we can use a much lower sampling rate.

Sampling

Undersampling
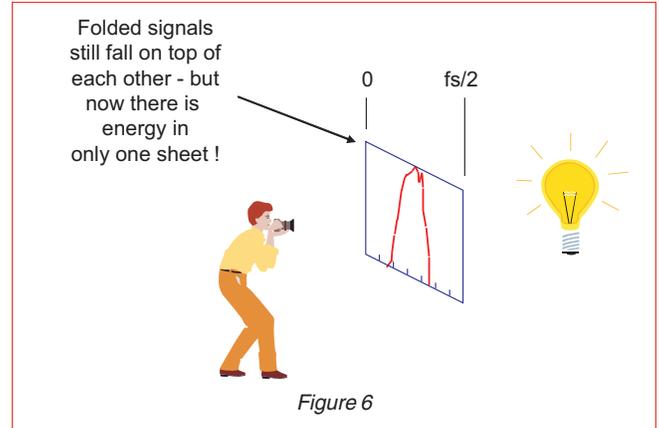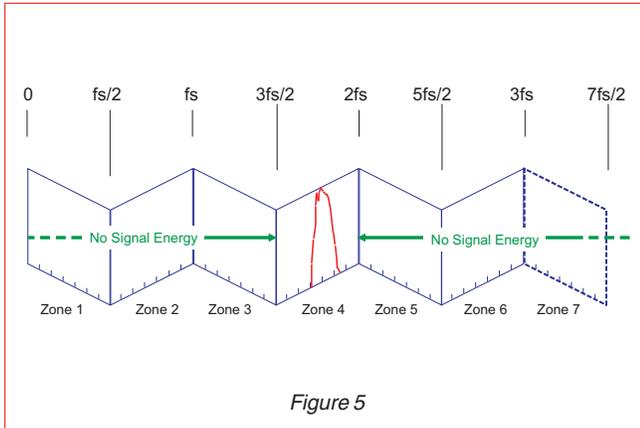
Figure 5

Figure 6

Undersampling allows us to use aliasing to our advantage, providing we follow the strict rules of the Nyquist Theorem.

In our previous IF signal example, suppose we try a sampling rate of 40 MHz.

Figure 5 shows a fan-fold paper plot with Fs = 40 MHz. You can see that zone 4 extends from 60 MHz to 80 MHz, nicely containing the entire IF signal band of 65 to 75 MHz.

Now when you collapse the fan fold sheets as shown in Figure 6, you can see that the IF signal is preserved after sampling because we have no signal energy in any other zone.

Also note that the odd zones fold with the lower frequency at the left (normal spectrum) and the even zones fold with the lower frequency at the right (reversed spectrum).

In this case, the signals from zone 4 are frequency-reversed. This is usually very easy to accommodate in the following stages of SDR systems.

The major rule to follow for successful undersampling is to make sure all of the energy falls entirely in one Nyquist zone.

There two ways to do this:
1. Insert a bandpass filter to eliminate all signals outside the one Nyquist zone.
2. Increase the sampling frequency so all signals fall entirely within one Nyquist zone.

Summary

Baseband sampling requires the sample frequency to be at least twice the signal bandwidth. This is the same as saying that all of the signals fall within the first Nyquist zone.

In real life, a good rule of thumb is to use the 80% relationship:

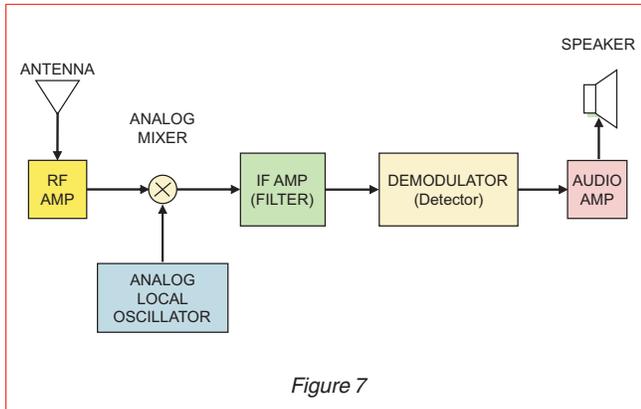$$Bandwidth = 0.8 \times f_s/2$$

Undersampling allows a lower sample rate even though signal frequencies are high, PROVIDED all of the signal energy falls within one Nyquist zone.

To repeat the Nyquist theorem: The sampling frequency must be at least twice the signal bandwidth — not the signal frequency.

Analog Radio Receiver Block Diagram

Figure 7

Analog Radio Receiver Mixer

Figure 8

The conventional heterodyne radio receiver shown in Figure 7, has been in use for nearly a century. Let's review the structure of the analog receiver so comparison to a digital receiver becomes apparent.

First the RF signal from the antenna is amplified, typically with a tuned RF stage that amplifies a region of the frequency band of interest.

This amplified RF signal is then fed into a mixer stage. The other input to the mixer comes from the local oscillator whose frequency is determined by the tuning control of the radio.
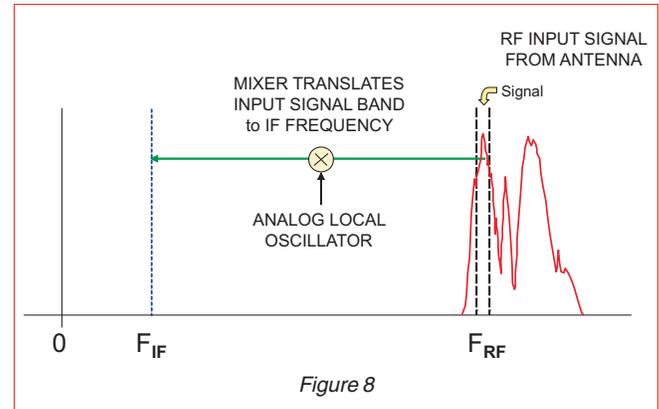
The mixer translates the desired input signal to the IF (Intermediate Frequency) as shown in Figure 8.

The IF stage is a bandpass amplifier that only lets one signal or radio station through. Common center frequencies for IF stages are 455 kHz and 10.7 MHz for commercial AM and FM broadcasts.

The demodulator recovers the original modulating signal from the IF output using one of several different schemes.

For example, AM uses an envelope detector and FM uses a frequency discriminator. In a typical home radio, the demodulated output is fed to an audio power amplifier which drives a speaker.

The mixer performs an analog multiplication of the two inputs and generates a difference frequency signal.

The frequency of the local oscillator is set so that the difference between the local oscillator frequency and the desired input signal (the radio station you want to receive) equals the IF.

For example, if you wanted to receive an FM station at 100.7 MHz and the IF is 10.7 MHz, you would tune the local oscillator to:

$$100.7 - 10.7 = 90 \text{ MHz}$$

This is called "downconversion" or "translation" because a signal at a high frequency is shifted down to a lower frequency by the mixer.

The IF stage acts as a narrowband filter which only passes a "slice" of the translated RF input. The bandwidth of the IF stage is equal to the bandwidth of the signal (or the "radio station") that you are trying to receive.

For commercial FM, the bandwidth is about 100 kHz and for AM it is about 5 kHz. This is consistent with channel spacings of 200 kHz and 10 kHz, respectively.

Principles of SDR

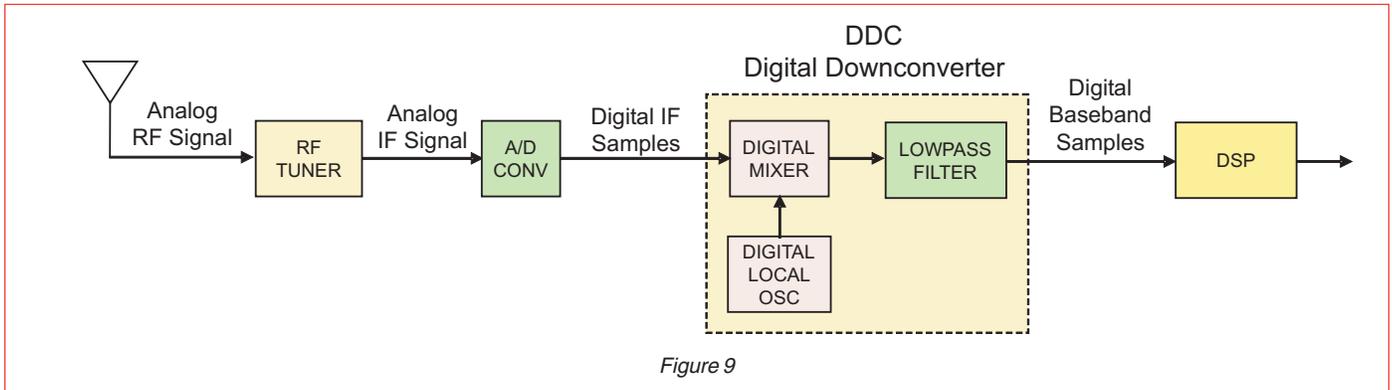## SDR Receiver Block Diagram

Figure 9

Figure 9 shows a block diagram of a software defined radio receiver. The RF tuner converts analog RF signals to analog IF frequencies, the same as the first three stages of the analog receiver.

The A/D converter that follows digitizes the IF signal thereby converting it into digital samples. These samples are fed to the next stage which is the digital downconverter (DDC) shown within the dotted lines.

The digital downconverter is typically a single monolithic chip or FPGA IP, and it is a key part of the SDR system.

A conventional DDC has three major sections:

- **A digital mixer**
- **A digital local oscillator**
- **An FIR lowpass filter**

The digital mixer and local oscillator translate the digital IF samples down to baseband. The FIR lowpass filter limits the signal bandwidth and acts as a decimating lowpass filter. The digital downconverter includes a lot of hardware multipliers, adders and shift register memories to get the job done.

The digital baseband samples are then fed to a block labeled DSP which performs tasks such as demodulation, decoding and other processing tasks.

Traditionally, these needs have been handled with dedicated application-specific ICs (ASICs), and programmable DSPs.

SDR Receiver Mixer
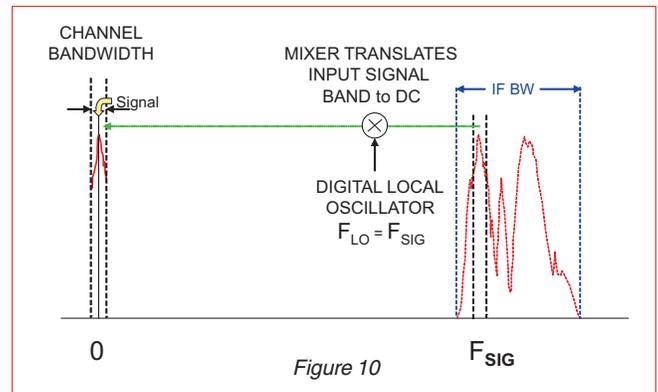
Figure 10

At the output of the mixer, the high frequency wideband signals from the A/D input (shown in Figure 10 above) have been translated down to DC as complex I and Q components with a frequency shift equal to the local oscillator frequency.

This is similar to the analog receiver mixer except *there*, the mixing was done down to an IF frequency. *Here*, the complex representation of the signal allows us to go right down to DC.

By tuning the local oscillator over its range, any portion of the RF input signal can be mixed down to DC.

In effect, the wideband RF signal spectrum can be "slid" around 0 Hz, left and right, simply by tuning the local oscillator. Note that upper and lower sidebands are preserved.

Principles of SDR

DDC Local Oscillator and Decimation

Figure 11A Local Oscillator Frequency Switching

F1   F2   F3

A/D Sample Rate
(before decimation)
Sample Rate: Fs

Decimated
Filter Output
Sample Rate: Fs/N

Figure 11B FIR Filter Decimation
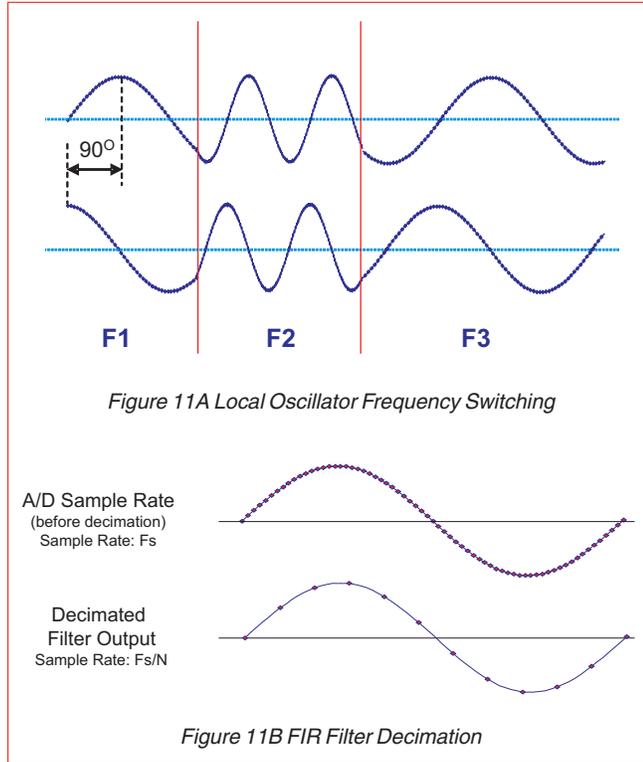
Because the local oscillator uses a digital phase accumulator, it has some very nice features. It switches between frequencies with phase continuity, so you can generate FSK signals or sweeps very precisely with no transients as shown in Figure 11A.

The frequency accuracy and stability are determined entirely by the A/D clock so it's inherently synchronous to the sampling frequency. There is no aging, drift or calibration since it's implemented entirely with digital logic.

Since the output of the FIR filter is band-limited, the Nyquist theorem allows us to lower the sample rate. If we are keeping only one out of every N samples, as shown in Figure 11B above, we have dropped the sampling rate by a factor of N.

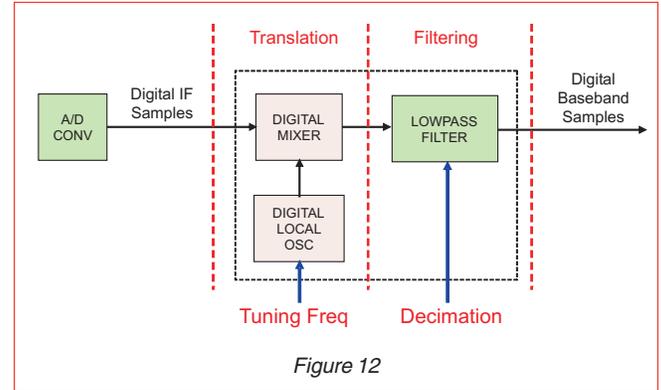## DDC Signal Processing

Figure 12

This process is called *decimation* and it means keeping one out of every N signal samples. If the decimated output sample rate is kept higher than twice the output bandwidth, no information is lost.

The clear benefit is that decimated signals can be processed easier, can be transmitted at a lower rate, or stored in less memory. As a result, decimation can dramatically reduce system costs!

As shown in Figure 12, the DDC performs two signal processing operations:

1. Frequency translation with the tuning controlled by the local oscillator.

2. Lowpass filtering with the bandwidth controlled by the decimation setting.

We will next turn our attention to the Software-Defined Radio Transmitter.

SDR Transmitter Block Diagram
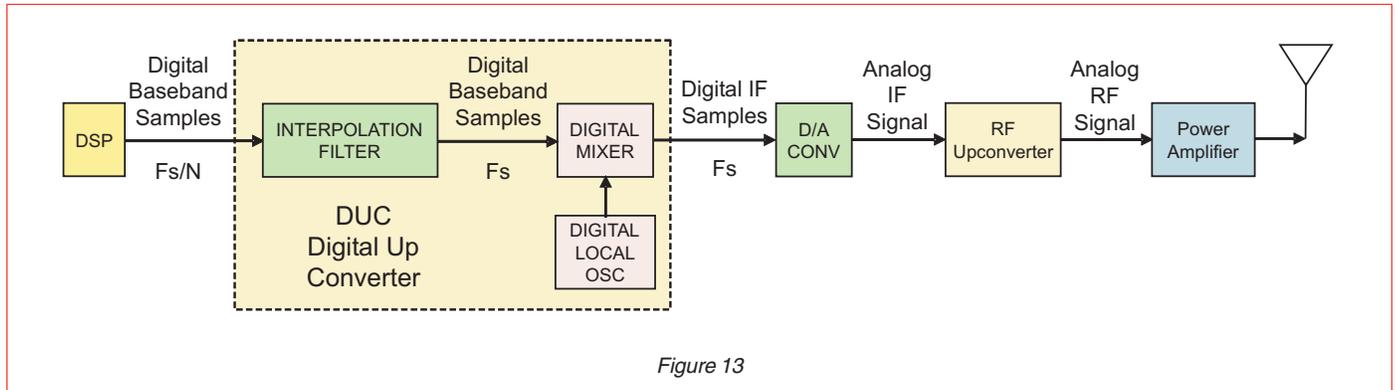
Figure 13

The input to the transmit side of an SDR system is a digital baseband signal, typically generated by a DSP stage as shown in Figure 13 above.

The digital hardware block in the dotted lines is a DUC (digital upconverter) that translates the baseband signal to the IF frequency.

The D/A converter that follows converts the digital IF samples into the analog IF signal.

Next, the RF upconverter converts the analog IF signal to RF frequencies.

Finally, the power amplifier boosts signal energy to the antenna.

DUC Signal Processing
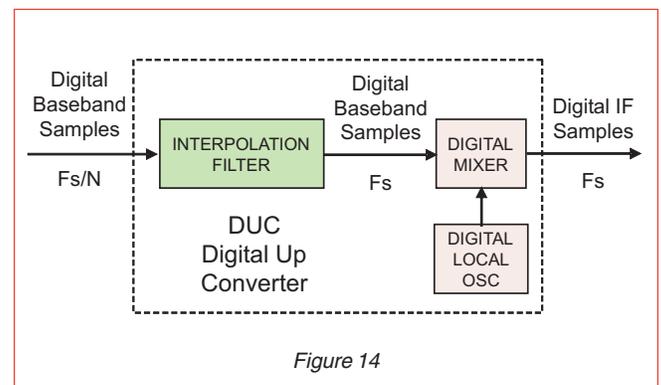
Figure 14

Inside the DUC shown in Figure 14, the digital mixer and local oscillator at the right translate baseband samples up to the IF frequency. The IF translation frequency is determined by the local oscillator.

The mixer generates one output sample for each of its two input samples. And, the sample frequency at the mixer output must be equal to the D/A sample frequency f_s.

Therefore, the local oscillator sample rate and the baseband sample rate must be equal to the D/A sample frequency f_s.

The local oscillator already operates at a sample rate of f_s, but the input baseband sample frequency at the left is usually much lower. This problem is solved with the *Interpolation Filter.*

Interpolation Filter: Time domain

Figure 15

Interpolation Filter: Frequency Domain

Figure 16
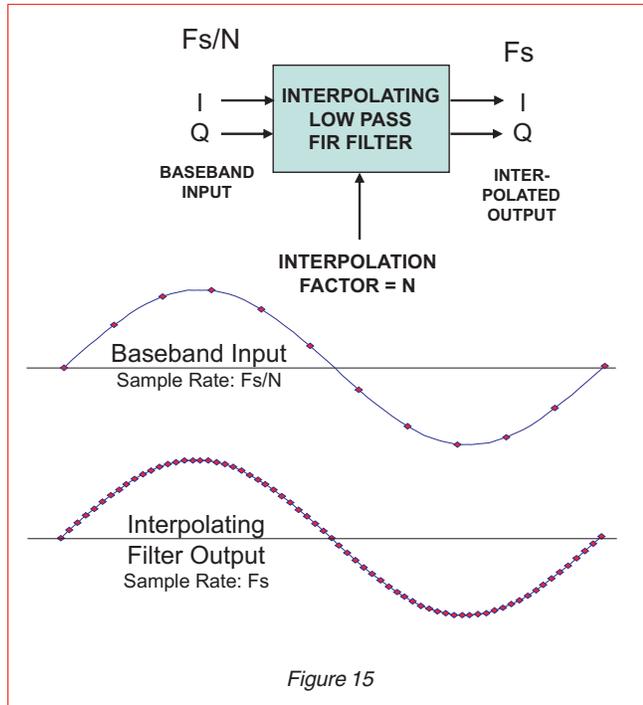
The interpolation filter must boost the baseband input sample frequency of f_s/N up to the required mixer input and D/A output sample frequency of f_s.

The interpolation filter increases the sample frequency of the baseband input signal by a factor N, known as the interpolation factor.

At the bottom of Figure 15, the effect of the interpolation filter is shown in the time domain.

Notice the baseband signal frequency content is completely preserved by filling in additional samples in the spaces between the original input samples.

The signal processing operation performed by the interpolation filter is the inverse of the decimation filter we discussed previously in the DDC section.

Figure 16 is a frequency domain view of the digital upconversion process.

This is exactly the opposite of the frequency domain view of the DDC in Figure 10.

The local oscillator setting is set equal to the required IF signal frequency, just as with the DDC.

DDC Processing

Figure 17
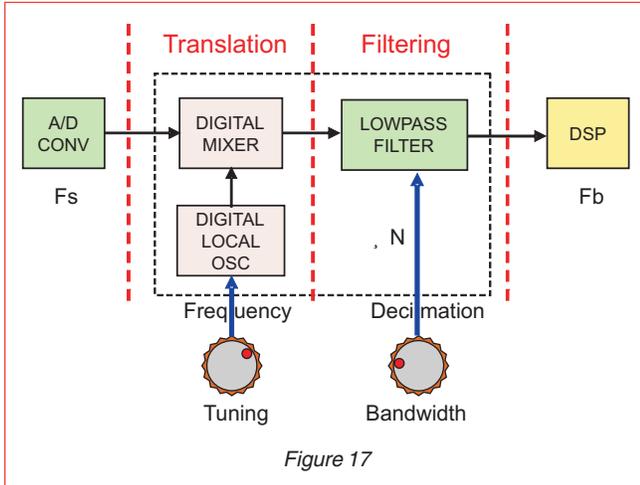
DUC Processing

Figure 18

Figure 17 shows the two-step processing performed by the digital downconverter.

Frequency translation from IF down to baseband is performed by the local oscillator and mixer.

The "tuning knob" represents the programmability of the local oscillator frequency to select the desired signal for downconversion to baseband.

The baseband signal bandwidth is set by setting decimation factor N and the lowpass FIR filter:

- Baseband sample frequency $f_b = f_s/N$
- Baseband bandwidth = 0.8 x f_b

The baseband bandwidth equation reflects a typical 80% passband characteristic, and complex (I+Q) samples.

The "bandwidth knob" represents the programmability of the decimation factor to select the desired baseband signal bandwidth.
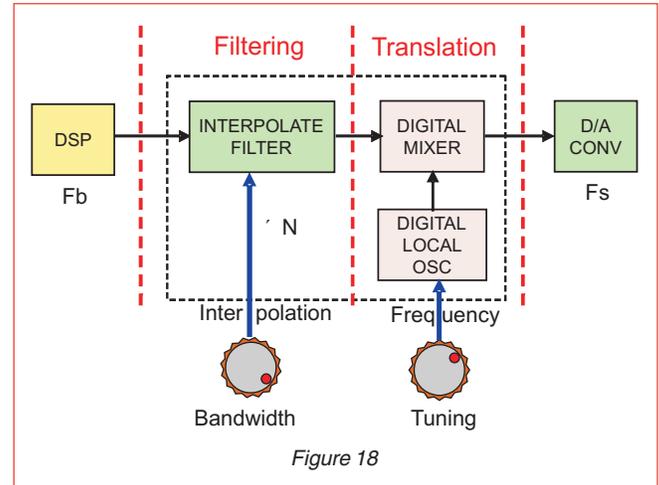
Figure 18 shows the two-step processing performed by the digital upconverter:

The ratio between the required output sample rate and the sample rate input baseband sample rate determines the interpolation factor N.

- Baseband bandwidth = 0.8 x f_b
- Output sample frequency $f_s = f_b$ x N

Again, the bandwidth equation assumes a complex (I+Q) baseband input and an 80% filter.

The "bandwidth knob" represents the programmability of the interpolation factor to select the desired input baseband signal bandwidth.

Frequency translation from baseband up to IF is performed by the local oscillator and mixer.

The "tuning knob" represents the programmability of the local oscillator frequency to select the desired IF frequency for translation up from baseband.

Key DDC and DUC Benefits

Figure 19

SDR Tasks
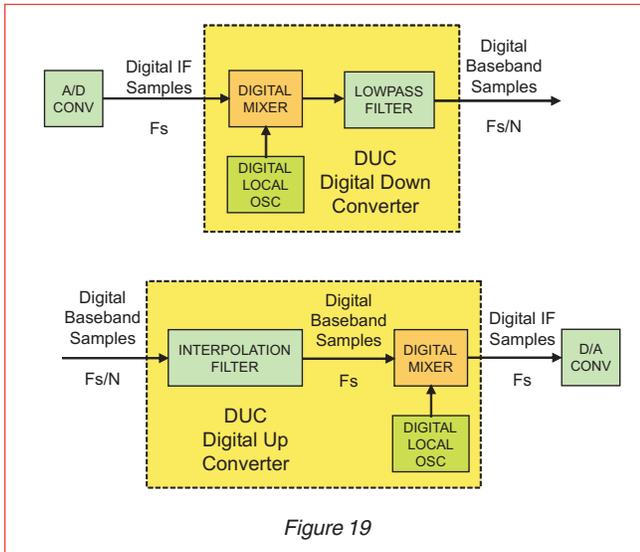
Figure 20

Think of the DDC as a hardware preprocessor for programmable DSP or GPP processor. It preselects only the signals you are interested in and removes all others. This provides an optimum bandwidth and minimum sampling rate into the processor.

The same applies to the DUC. The processor only needs to generate and deliver the baseband signals sampled at the baseband sample rate. The DUC then boosts the sampling rate in the interpolation filter, performs digital frequency translation, and delivers samples to the D/A at a very high sample rate.

The number of processors required in a system is directly proportional to the sampling frequency of input and output data. As a result, by reducing the sampling frequency, you can dramatically reduce the cost and complexity of the programmable DSPs or GPPs in your system.

Not only do DDCs and DUCs reduce the processor workload, the reduction of bandwidth and sampling rate helps save time in data transfers to another subsystem. This helps minimize recording time and disk space, and reduces traffic and bandwidth across communication channels.
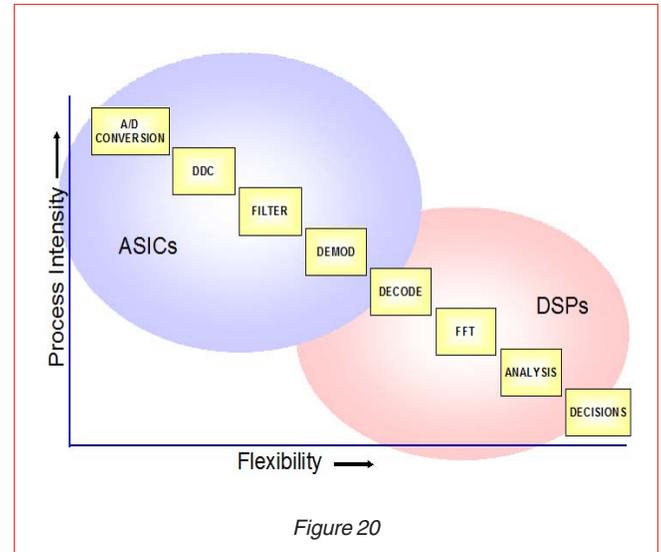
Here we've ranked some of the popular signal processing tasks associated with SDR systems on a two axis graph, with computational Processing Intensity on the vertical axis and Flexibility on the horizontal axis.

What we mean by process intensity is the degree of highly-repetitive and rather primitive operations. At the upper left, are dedicated functions like A/D converters and DDCs that require specialized hardware structures to complete the operations in real time. ASICs are usually chosen for these functions.

Flexibility pertains to the uniqueness or variability of the processing and how likely the function may have to be changed or customized for any specific application. At the lower right are tasks like analysis and decision making which are highly variable and often subjective.

Programmable general-purpose processors or DSPs are usually chosen for these tasks since these tasks can be easily changed by software.

Now let's temporarily step away from the software radio tasks and take a deeper look at programmable logic devices.

Technology

Early Roles for FPGAs

- Used primarily to replace discrete digital hardware circuitry for:
  - Control logic
  - Glue logic
  - Registers and gates
  - State machines
  - Counters and dividers
- Devices were selected by hardware engineers
- Programmed functions were seldom changed after the design went into production

Figure 21

Legacy FPGA Design Methodologies

- Tools were oriented to hardware engineers
  - Schematic processors
  - Boolean processors
  - Gates, registers, counters, multipliers
- Successful designs required high-level hardware engineering skills for:
  - Critical paths and propagation delays
  - Pin assignment and pin locking
  - Signal loading and drive capabilities
  - Clock distribution
  - Input signal synchronization and skew analysis

Figure 22

As true programmable gate functions became available in the 1970's, they were used extensively by hardware engineers to replace control logic, registers, gates, and state machines which otherwise would have required many discrete, dedicated ICs.

Often these programmable logic devices were one-time factory-programmed parts that were soldered down and never changed after the design went into production.

These programmable logic devices were mostly the domain of hardware engineers and the software tools were tailored to meet their needs. You had tools for accepting boolean equations or even schematics to help generate the interconnect pattern for the growing number of gates.

Then, programmable logic vendors started offering predefined logic blocks for flip-flops, registers and counters that gave the engineer a leg up on popular hardware functions.

Nevertheless, the hardware engineer was still intimately involved with testing and evaluating the design using the same skills he needed for testing discrete logic designs. He had to worry about propagation delays, loading, clocking and synchronizing—all tricky problems that usually had to be solved the hard way—with oscilloscopes or logic analyzers.

FPGAs: New Device Technology

- ◆ 500+ MHz DSP Slices and Memory Structures
- ◆ Over 3500 dedicated on-chip hardware multipliers
- ◆ On-board GHz Serial Transceivers
- ◆ Partial Reconfigurability Maintains
- ◆ Operation During Changes
- ◆ Switched Fabric Interface Engines
- ◆ Over 690,000 Logic Cells
- ◆ Gigabit Ethernet media access controllers
- ◆ On-chip 405 PowerPC RISC micro-controller cores
- ◆ Memory densities approaching 85 million bits
- ◆ Reduced power with core voltages at 1 volt
- ◆ Silicon geometries to 28 nanometers
- ◆ High-density BGA and flip-chip packaging
- ◆ Over 1200 user I/O pins
- ◆ Configurable logic and I/O interface standards

Figure 23

FPGAs: New Development Tools

- ■ High Level Design Tools
  - • Block Diagram System Generators
  - • Schematic Processors
  - • High-level language compilers for VHDL & Verilog
  - • Advanced simulation tools for modeling speed, propagation delays, skew and board layout
  - • Faster compilers and simulators save time
  - • Graphically-oriented debugging tools
- ■ IP (Intellectual Property) Cores
  - • FPGA vendors offer both free and licensed cores
  - • FPGA vendors promote third party core vendors
  - • Wide range of IP cores available

Figure 24

It's virtually impossible to keep up to date on FPGA technology, since new advancements are being made every day.

The hottest features are processor cores inside the chip, computation clocks to 500 MHz and above, and lower core voltages to keep power and heat down.

Several years ago, dedicated hardware multipliers started appearing and now you'll find literally thousands of them on-chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over ten million gates result from silicon geometries shrinking below 0.1 micron.

BGA and flip-chip packages provide plenty of I/O pins to support on-board gigabit serial transceivers and other user-configurable system interfaces.

New announcements seem to be coming out every day from chip vendors like Xilinx and Altera in a never-ending game of outperforming the competition.

To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

Excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This minimizes some of the tricky timing work for hardware engineers and can save one hours of tedious troubleshooting during design verification and production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer thousands of application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-to-market crunch and to minimize risk.

Technology

FPGAs for SDR

- Parallel Processing
- Hardware Multipliers for DSP
  - FPGAs can now have over 500 hardware multipliers
- Flexible Memory Structures
  - Dual port RAM, FIFOs, shift registers, look up tables, etc.
- Parallel and Pipelined Data Flow
  - Systolic simultaneous data movement
- Flexible I/O
  - Supports a variety of devices, buses and interface standards
- High Speed
- Available IP cores optimized for special functions

Figure 25

Like ASICs, all the logic elements in FPGAs can execute in parallel. This includes the hardware multipliers, and you can now get over 1000 of them on a single FPGA.

This is in sharp contrast to programmable DSPs, which normally have just a handful of multipliers that must be operated sequentially.

FPGA memory can now be configured with the design tool to implement just the right structure for tasks that include dual port RAM, FIFOs, shift registers and other popular memory types.

These memories can be distributed along the signal path or interspersed with the multipliers and math blocks, so that the whole signal processing task operates in parallel in a systolic pipelined fashion.

Again, this is dramatically different from sequential execution and data fetches from external memory as in a programmable DSP.

As we said, FPGAs now have specialized serial and parallel interfaces to match requirements for high-speed peripherals and buses.

FPGAs Bridge the SDR Application Space
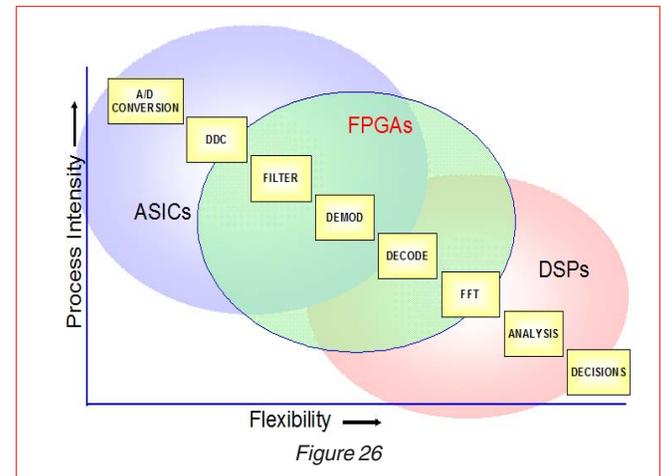
Figure 26

As a result, FPGAs have significantly invaded the application task space as shown by the center bubble in the task diagram above.

They offer the advantages of parallel hardware to handle some of the high process-intensity functions like DDCs and the benefit of programmability to accommodate some of the decoding and analysis functions of DSPs.

These advantages may come at the expense of increased power dissipation and increased product costs. However, these considerations are often secondary to the performance and capabilities of these remarkable devices.

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Typical Pentek Products with Factory-Installed SDR IP Cores

Model	Analog Channels	Sampling Freq (max)	Input Bits	DDC Channels	Decimation Range	Output Bits	DUC Channels	Interpol. Range	Beam-former
7142-428	4	125 MHz	14	4	2–64K	16 or 24	None	None	No
7151	4	200 MHz	16	256	128–1K	16 or 24	None	None	No
7152	4	200 MHz	16	32	16–8K	16 or 24	None	None	Yes
7153	4	200 MHz	16	2 or 4	2–64K/2–256	16 or 24	None	None	Yes
71621	3	200 MHz	16	3	2–64K	16 or 24	1	2–512K	Yes
71641	1 or 2	3.6 or 1.8 GHz	12	1 or 2	4, 8 or 16	16	None	None	No
71651	2	500/400 MHz	12/14	2	2–128K	16 or 24	1	2–512K	Yes
71661	4	200 MHz	16	4	2–64K	16 or 24	None	None	Yes
71662	4	200 MHz	16	32	16–8K	24	None	None	No
71671	None	None	–	None	–	16	4	2–1024K	No

Figure 27

The above chart shows the salient characteristics for some of Pentek's SDR products with factory-instlled IP cores. All these products are available off-the-self and are in the Pentek datasheets and catalogs.

The chart provides information regarding the number of input channels, maximum sampling frequency of their A/Ds, the number of bits, and number of DDC channels in each one. This information is followed by DDC characteristics such as number of DDC channels and the decimation range.

Other information that's specific to each core is included as well as an indication of the models that include an interpolation filter and output D/A. As shown in the chart, many of these models include features that are critical for beamforming and direction-finding applications.

All the models shown here are PMC or XMC modules. As with all Pentek SDR products, these models are also available in CompactPCI, PCI Express, OpenVPX, and AMC formats as well.

FPGA Resource Comparison

	Virtex-II Pro VP	Virtex-4 FX, LX, SX	Virtex-5 LX, SX	Virtex-6 LX, SX	Virtex-7 VX
Logic Cells	53K–74K	55K–110K	52K–155K	128K–314K	326K–693K
Slices*	23K–33K	24K–49K	8K–24K	20K–49K	51K–108K
CLB Flip-Flops	46K–66K	48K–98K	32K–96K	160K–392K	408K–864K
Block RAM (kb)	4,176–5,904	4,176–6,768	4,752–8,784	9,504–25,344	27,000–52,920
DSP Hard IP	18x18 Multipliers	DSP48	DSP48E	DSP48E	DSP48E
DSP Slices	232–328	96–512	128–640	480–1,344	1,120–3,600
Serial Gbit Transceivers	N/A	0–20	12–16	20–24	28–80
PCI Express Support	N/A	N/A	N/A	Gen 2 x8	Gen 2 x8, Gen 3 x8
User I/O	852–996	576–960	480–680	600–720	700–1,000

*Virtex-II Pro and Virtex-4 Slices actually require 2.25 Logic Cells;
*Virtex-5, Virtex-6 and Virtex-7 Slices actually require 6.4 Logic Cells

Figure 28

The above chart compares the available resources in the five Xilinx FPGA families that are used in most of the Pentek products.
- Virtex-II Pro: VP
- Virtex-4: FX, LX and SX
- Virtex-5: LX and SX
- Virtex-6: LX and SX
- Virtex-7: VX

The Virtex-II family includes hardware multipliers that support digital filters, averagers, demodulators and FFTs—a major benefit for software radio signal processing. The Virtex-II Pro family dramatically increased the number of hardware multipliers and also added embedded PowerPC microcontrollers.

The Virtex-4 family is offered as three subfamilies that dramatically boost clock speeds and reduce power dissipation over previous generations.

The Virtex-4 LX family delivers maximum logic and I/O pins while the SX family boasts of 512 DSP slices for maximum DSP performance. The FX family is a generous mix of all resources and is the only family to offer RocketIO, PowerPC cores, and the newly added gigabit Ethernet ports.

The Virtex-5 family LX devices offer maximum logic resources, gigabit serial transceivers, and Ethernet media access controllers. The SX devices push DSP capabilities with all of the same extras as the LX.

The Virtex-5 devices offer lower power dissipation, faster clock speeds and enhanced logic slices. They also improve the clocking features to handle faster memory and gigabit interfaces. They support faster single-ended and differential parallel I/O buses to handle faster peripheral devices.

The Virtex-6 and Virtex-7 devices offer still higher density, more processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements including PCI Express. Virtex-6 supports PCIe 2.0 and Virtex-7 supports PCIe 3.0

The ample DSP slices are responsible for the majority of the processing power of the Virtex-6 and Virtex-7 families. Increases in operating speed from 500 MHz in V-4, to 550 MHz in V-5, to 600 MHz in V-6, to 900 MHz in V-7 and continuously increasing density allow more DSP slices to be included in the same-size package. As shown in the chart, Virtex-6 tops out at an impressive 1,344 DSP slices, while Virtex-7 tops out at an even more impressive 3,600 DSP slices.

PMC, XMC, CompactPCI, PCI, PCI Express, OpenVPX, AMC, and VMEbus Software Radio

PMC/XMC Module

6U CompactPCI Board

3U OpenVPX Boards COTS and Rugged

Half-length PCI Express Board

AMC Board

PCI Board

Full-length PCI Express Board

VMEbus Board

Figure 29
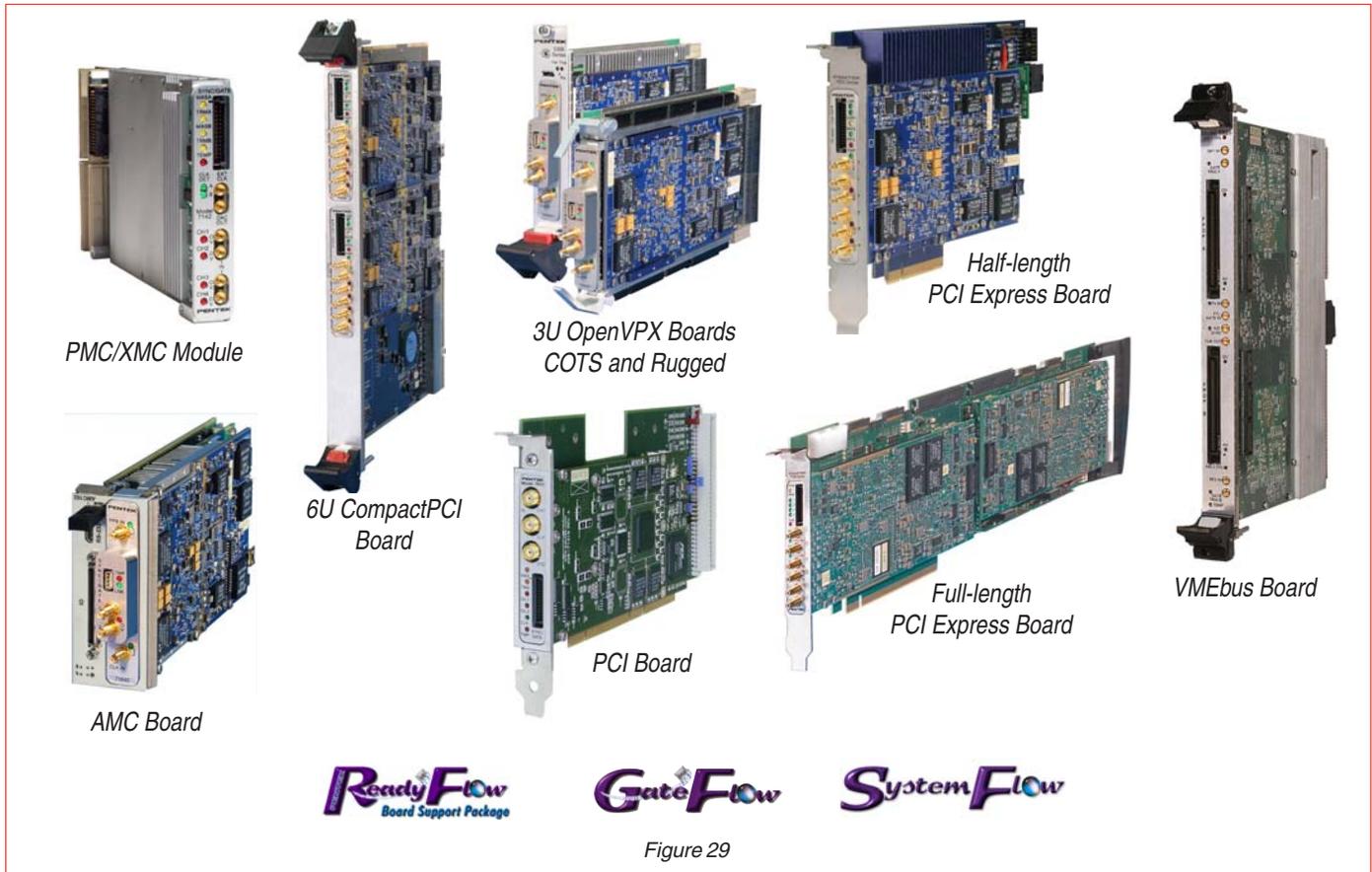
The Pentek family of board-level software radio products is the most comprehensive in the industry. Most of these products are available in several formats to satisfy a wide range of requirements.

In addition to their commercial versions, many software radio products are available in ruggedized and conduction-cooled versions.

Most of the software radio products include input A/D converters. Some of these products are software radio receivers in that they include only DDCs. Others are software radio transceivers and they include DDCs as well as DUCs with output D/A converters. These come with independent input and output clocks.

All Pentek software radio products include multiboard synchronization that facilitates the design of multichannel systems with synchronous clocking, gating and triggering.

Pentek's comprehensive software support includes the ReadyFlow® Board Support Package, the GateFlow® FPGA Design Kit and high-performance factory-installed IP cores that expand the features and range of many Pentek software radio products. In addition, Pentek high-speed recording systems are supported with SystemFlow® recording software that features a graphical user interface.

In addition to product overviews presented in the pages that follow, a complete listing of these products with active links to their datasheets on Pentek's website is included at the end of this handbook.

Multichannel Transceivers with Virtex-4 FPGAs

Model 7142 PMC/XMC • Model 7242 6U cPCI • Model 7342 3U cPCI • Model 7642 PCI
Model 7742 Full-length PCIe • Model 7842 Half-length PCIe • Model 5342 3U VPX
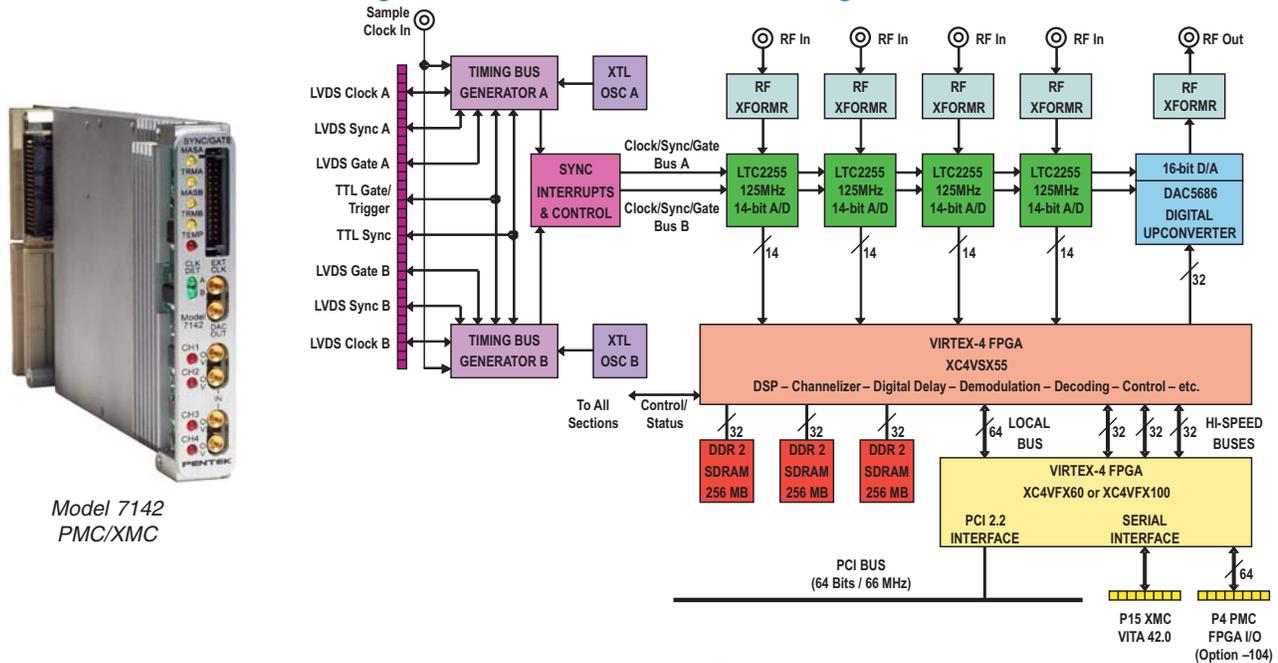
Model 7142
PMC/XMC

Figure 30

The Model 7142 is a Multichannel PMC/XMC module. It includes four 125 MHz 14-bit A/D converters and one upconverter with a 500 MHz 16-bit D/A converter to support wideband receive and transmit communication channels.

Two Xilinx Virtex-4 FPGAs are included: an XC4VSX55 or LX100 and an XC4VFX60 or FX100. The first FPGA is used for control and signal processing functions, while the second one is used for implementing board interface functions including the XMC interface.

It also features 768 MB of SDRAM for implementing up to 2.0 sec of transient capture or digital delay memory for signal intelligence tracking applications at 125 MHz.

A 16 MB flash memory supports the boot code for the two on-board IBM 405 PowerPC microcontroller cores within the FPGA.

A 9-channel DMA controller and 64 bit / 66 MHz PCI interface assures efficient transfers to and from the module.

A high-performance 160 MHz IP core wideband digital downconverter may be factory-installed in the first FPGA.

Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the second FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D and D/A converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7142 are also available as a PCIe full-length board (Models 7742 and 7742D dual density), PCIe half-length board (Model 7842), 3U VPX (Model 5342), PCI board (Model 7642), 6U cPCI (Models 7242 and 7242D dual density), and 3U cPCI (Model 7342).

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Products

Transceivers with Four Multiband DDCs and Interpolation Filter Installed Cores

Model 7142-428 PMC/XMC • Model 7242-428 6U cPCI • Model 7342-428 3U cPCI
Model 7642-428 PCI • Model 7742-428 Full-length PCIe
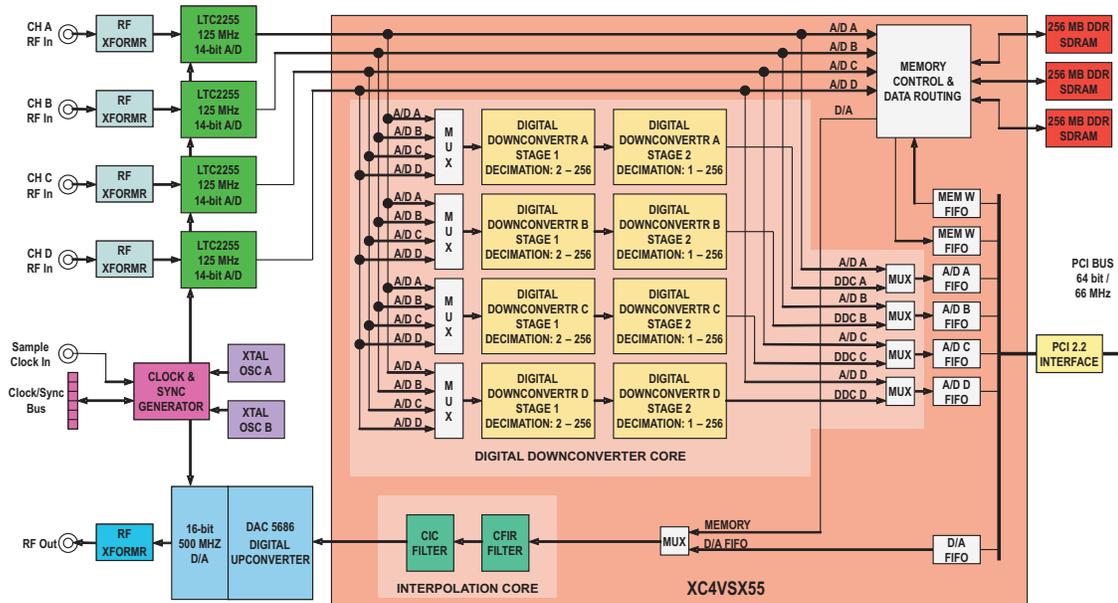Model 7742-428 Half-length PCIe • Model 5342-428 3U VPX

Figure 31

The Pentek IP Core 428 includes four high-performance multiband DDCs and an interpolation filter. Factory-installed in the Model 7142 FPGA, they add DDCs to the Model 7142 and extend the range of its DAC5686 DUC.

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The DDCs consist of two cascaded decimating FIR filters. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain may be used to amplify small signals after out-of-band signals have been filtered out.

The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable by using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7142-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overal decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, for a maximum interpolation of 32,768.

Versions of the 7142-428 are also available as a PCIe full-length board (Models 7742-428 and 7742D-428 dual density), PCIe half-length board (Model 7842-428), PCI board (Model 7642-428), 6U cPCI (Models 7242-428 and 7242D-428 dual density), 3U cPCI (Model 7342-428), and 3U VPX (Model 5342-428).

Products

Quad 200 MHz 16-bit A/D with Virtex-5 FPGAs

Model 7150 PMC/XMC • Model 7250 6U cPCI • Model 7350 3U cPCI • Model 7650 PCI
Model 7750 Full-length PCIe • Model 7850 Half-length PCIe • Model 5350 3U VPX
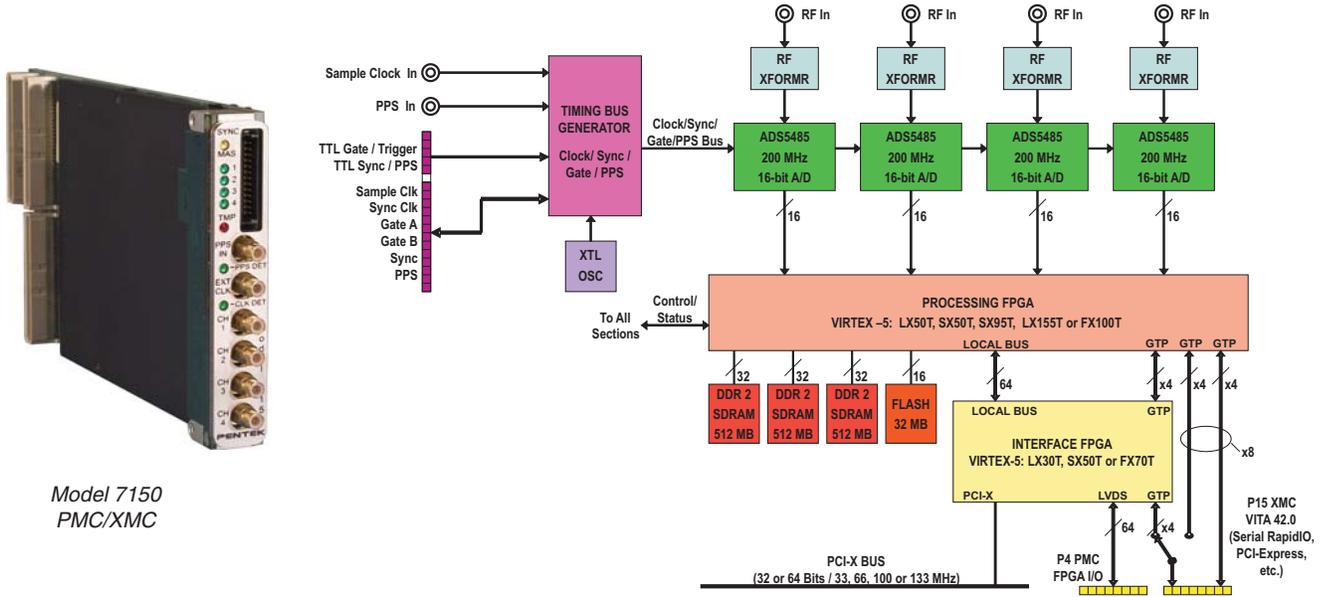
Model 7150
PMC/XMC

Figure 32

Model 7150 is a quad, high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds supported by an array of data processing and transport resources ideally matched to the requirements of high-performance systems. Model 7150 uses the popular PMC format and supports the emerging VITA 42 XMC standard for switched fabric interfaces.

The Model 7150 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Three independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 9-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7150 are also available as a PCIe full-length board (Models 7750 and 7750D dual density), PCIe half-length board (Model 7850), PCI board (Model 7650), 6U cPCI (Models 7250 and 7250D dual density), 3U cPCI (Model 7350), and 3U VPX (Model 5350).

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Products

256-Channel DDC Installed Core with Quad 200 MHz, 16-bit A/D

Model 7151 PMC • Model 7251 6U cPCI • Model 7351 3U cPCI • Model 7651 PCI
Model 7751 Full-length PCIe • Model 7851 Half-length PCIe • Model 5351 3U VPX

Figure 33
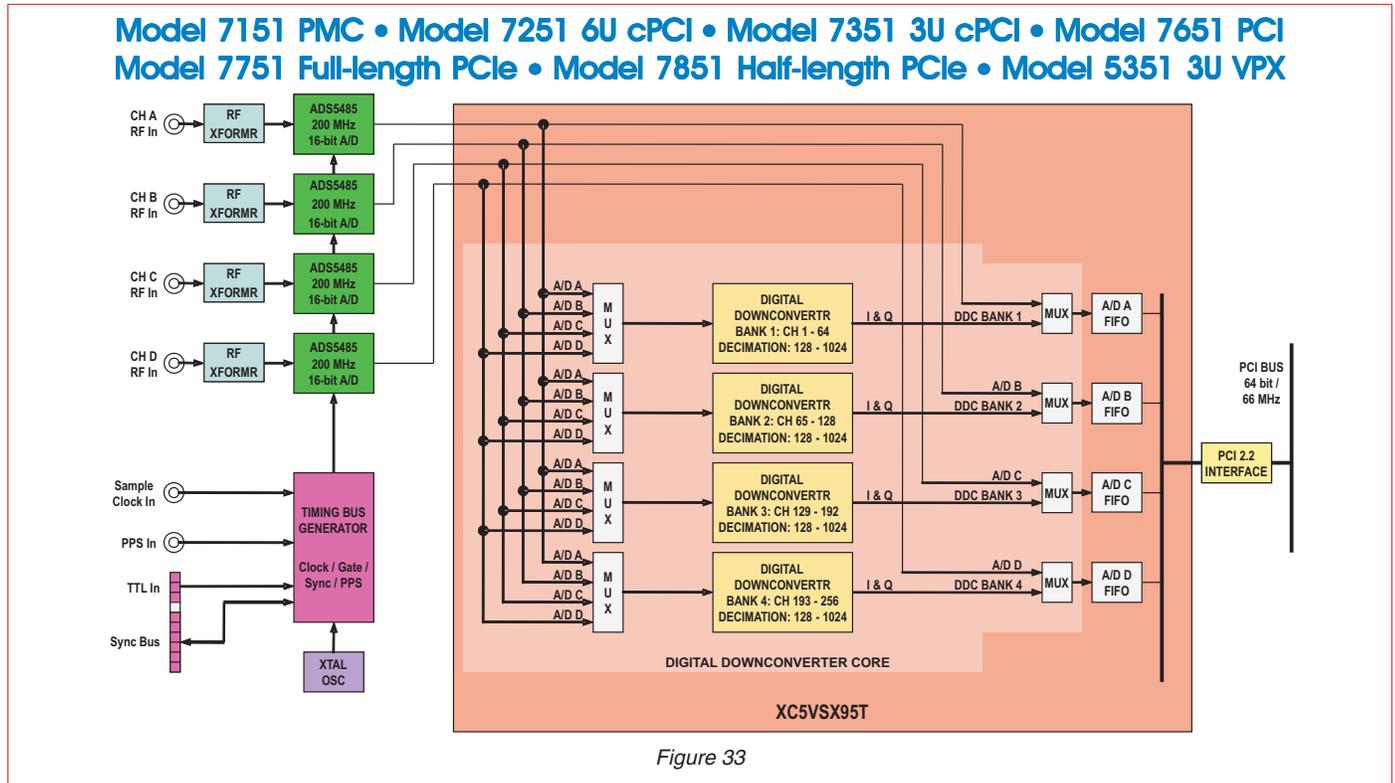
The Model 7151 PMC module is a 4-channel high-speed digitizer with a factory-installed 256-channel DDC core. The front end of the module accepts four RF inputs and transformer-couples them into four 16-bit A/D converters running at 200 MHz. The digitized output signals pass to a Virtex-5 FPGA for routing, formatting and DDC signal processing.

The Model 7151 employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 256 DDCs has an independent 32-bit tuning frequency setting.

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting

supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples. Any number of channels can be enabled within each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Versions of the 7151 are also available as a PCIe full-length board (Models 7751 and 7751D dual density), PCIe half-length board (Model 7851), PCI board (Model 7651), 6U cPCI (Models 7251 and 7251D dual density), 3U cPCI (Model 7351), and 3U VPX (Model 5351).

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Products

32-Channel DDC Installed Core with Quad 200 MHz, 16-bit A/D

Model 7152 PMC • Model 7252 6U cPCI • Model 7352 3U cPCI • Model 7652 PCI
Model 7752 Full-length PCIe • Model 7852 Half-length PCIe • Model 5352 3U VPX
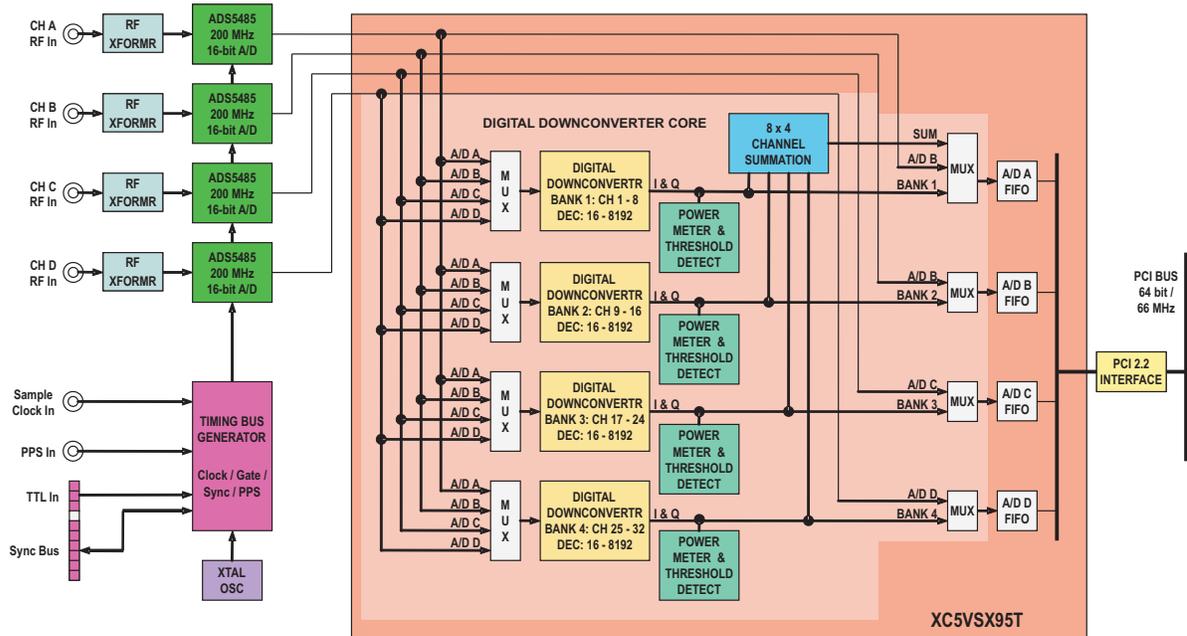

Figure 34

The Model 7152 PMC module is a 4-channel high-speed digitizer with a factory-installed 32-channel DDC core. The front end of the module accepts four RF inputs and transformer-couples them into four 16-bit A/D converters running at 200 MHz. The digitized output signals pass to a Virtex-5 FPGA for routing, formatting and DDC signal processing.

The Model 7152 employs an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 32 DDCs has an independent 32-bit tuning frequency setting.

All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can

have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output band-width is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank. Gain and phase control, power meters and threshold detectors are included.

Versions of the 7152 are also available as a PCIe full-length board (Models 7752 and 7752D dual density), PCIe half-length board (Model 7852), PCI board (Model 7652), 6U cPCI (Models 7252 and 7252D dual density), 3U cPCI (Model 7352), and 3U VPX (Model 5352).

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Products

4-Channel DDC and Beamformer Installed Core with four 200 MHz, 16-bit A/Ds

Model 7153 PMC/XMC • Model 7253 6U cPCI • Model 7353 3U cPCI • Model 7653 PCI
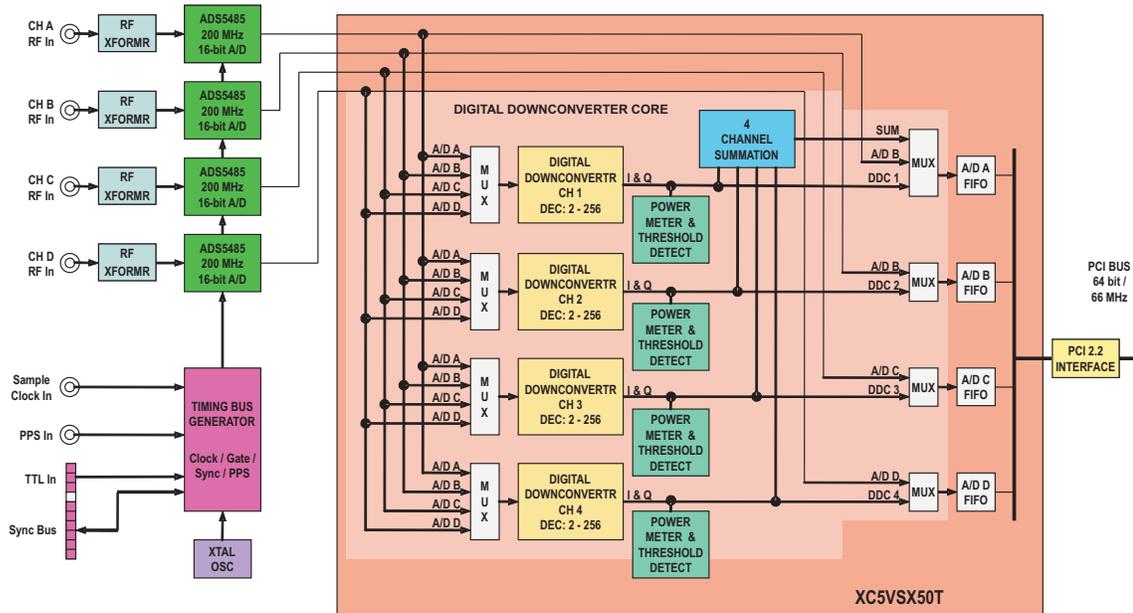### Model 7753 Full-length PCIe • Model 7853 Half-length PCIe • Model 5353 3U VPX

Figure 35

Model 7153 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel DDC (digital downconverter) installed core and a complete set of beamforming functions. With built-in multiboard synchronization and an Aurora gigabit serial interface, it provides everything needed for implementing multichannel beamforming systems.

The Model 7153 employs an advanced FPGA-based DDC engine consisting of four identical multiband banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 4 DDCs has an independent 32-bit tuning frequency setting.

All four DDCs have a decimation setting that can range from 2 to 256, programmable independently in steps of 1. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output band-width is better than 100 dB.

In addition to the DDCs, the 7153 features a complete beamforming subsystem. Each channel contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 ksamples. The power meters present average power measurements for each channel in easy-to-read registers. Each channel also includes a threshold detector that sends an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold.

Versions of the 7153 are also available as a PCIe full-length board (Models 7753 and 7753D dual density), PCIe half-length board (Model 7853), PCI board (Model 7653), 6U cPCI (Models 7253 and 7253D dual density), 3U cPCI (Model 7353), and 3U VPX (Model 5353).

Products

Dual SDR Transceivers with 400 MHz A/D, 800 MHz D/A, and Virtex-5 FPGAs

Model 7156 PMC/XMC • Model 7256 6U cPCI • Model 7356 3U cPCI • Model 7656 PCI
Model 7756 Full-length PCIe • Model 7856 Half-length PCIe • Model 5356 3U VPX

Model 7156 PMC/XMC

Figure 36

Model 7156 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 400 MHz 14-bit A/Ds, a DUC with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7156 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7156 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A high-performance IP core wideband DDC may be factory-installed in the processing FPGA.

A 5-channel DMA controller and 64 bit/100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7156 are also available as a PCIe full-length board (Models 7756 and 7756D dual density), PCIe half-length board (Model 7856), PCI board (Model 7656), 6U cPCI (Models 7256 and 7256D dual density), 3U cPCI (Model 7356), and 3U VPX (Model 5356). All these products have similar features.

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Dual SDR Transceivers with 500 MHz A/D, 800 MHz D/A, and Virtex-5 FPGAs

Model 7158 PMC/XMC • Model 7258 6U cPCI • Model 7358 3U cPCI • Model 7658 PCI
Model 7758 Full-length PCIe • Model 7858 Half-length PCIe • Model 5358 3U VPX
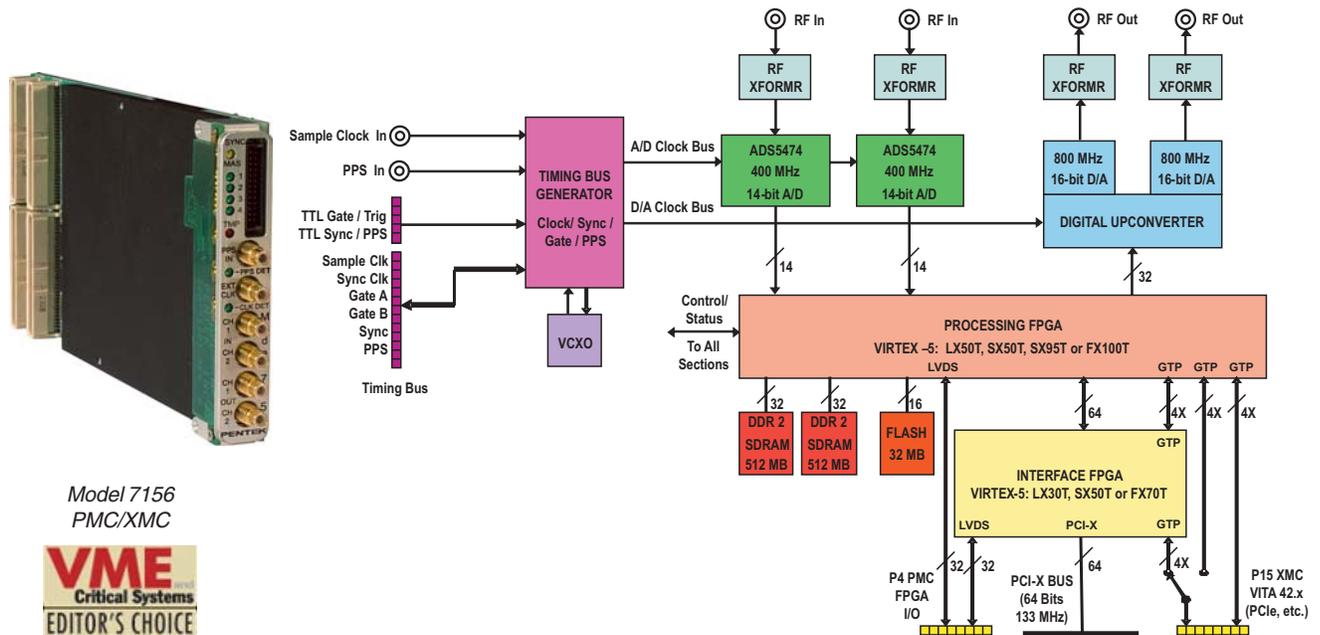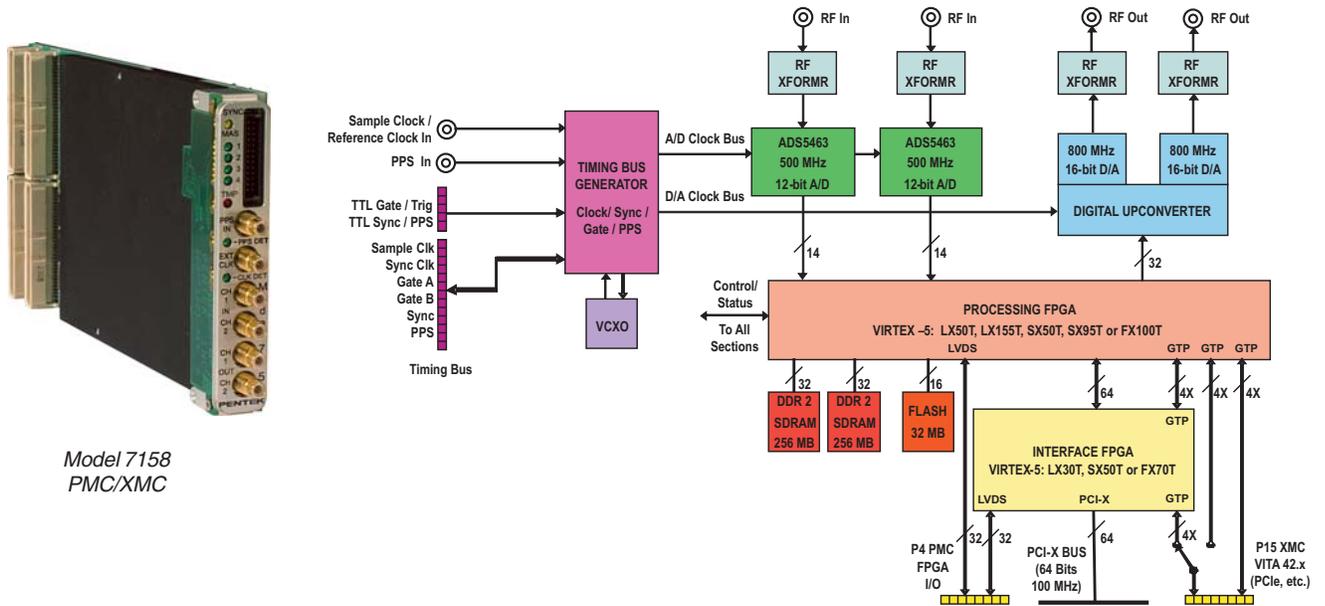

Model 7158 PMC/XMC

Figure 37

Model 7158 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 500 MHz 12-bit A/Ds, a digital upconverter with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7158 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7158 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 256 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 5-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7158 are also available as a PCIe full-length board (Models 7758 and 7758D dual density), PCIe half-length board (Model 7858), PCI board (Model 7658), 6U cPCI (Models 7258 and 7258D dual density), 3U cPCI (Model 7358), and 3U VPX (Model 5358). All these products have similar features.

Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA

Model 71620 XMC • Model 78620 PCIe • Model 53620 3U VPX • Model 56620 AMC
Model 72620 6U cPCI • Model 73620 3U cPCI • Model 74620 6U cPCI

Model 71620 XMC

Figure 38

Model 71620 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71620 includes general purpose and gigabit serial connectors for application-specific I/O .

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71620 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 71620 are also available as a PCIe half-length board (Model 78620), 3U VPX (Model 53620), AMC (Model 56620), 6U cPCI (Models 72620 and 74620 with dual density), and 3U cPCI (Model 73620).

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Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA

Model 71720 XMC • Model 78720 PCIe • Model 53720 3U VPX • Model 56720 AMC
Model 72720 6U cPCI • Model 73720 3U cPCI • Model 74720 6U cPCI
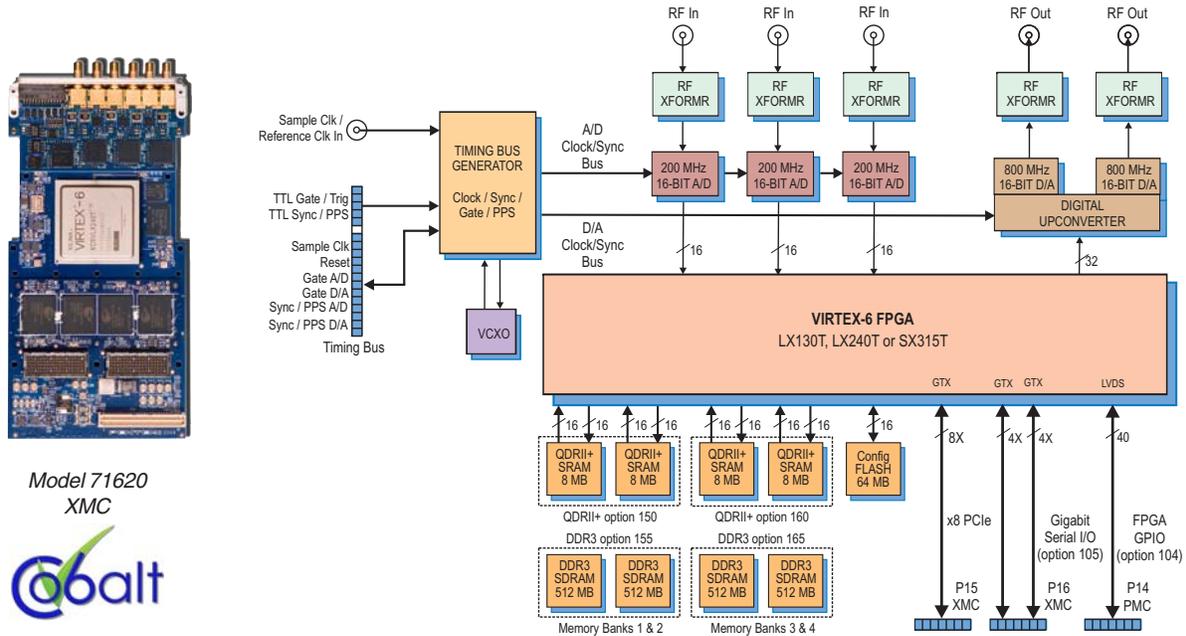

Model 71720 XMC

Onyx

GateXpress

Figure 39

Model 71720 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71720 includes general-purpose and gigabit-serial connectors for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

Multiple 71720's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Versions of the 71720 are also available as a PCIe half-length board (Model 78720), 3U VPX (Model 53720), AMC (Model 56720), 6U cPCI (Models 72720 and 74720 with dual density), and 3U cPCI (Model 73720).

GateXpress™ is a sophisticated configuration manager for loading and reloading the Virtex-7 FPGA. More information is available in the next page.

Products

GateXpress for FPGA-PCIe Configuration Management
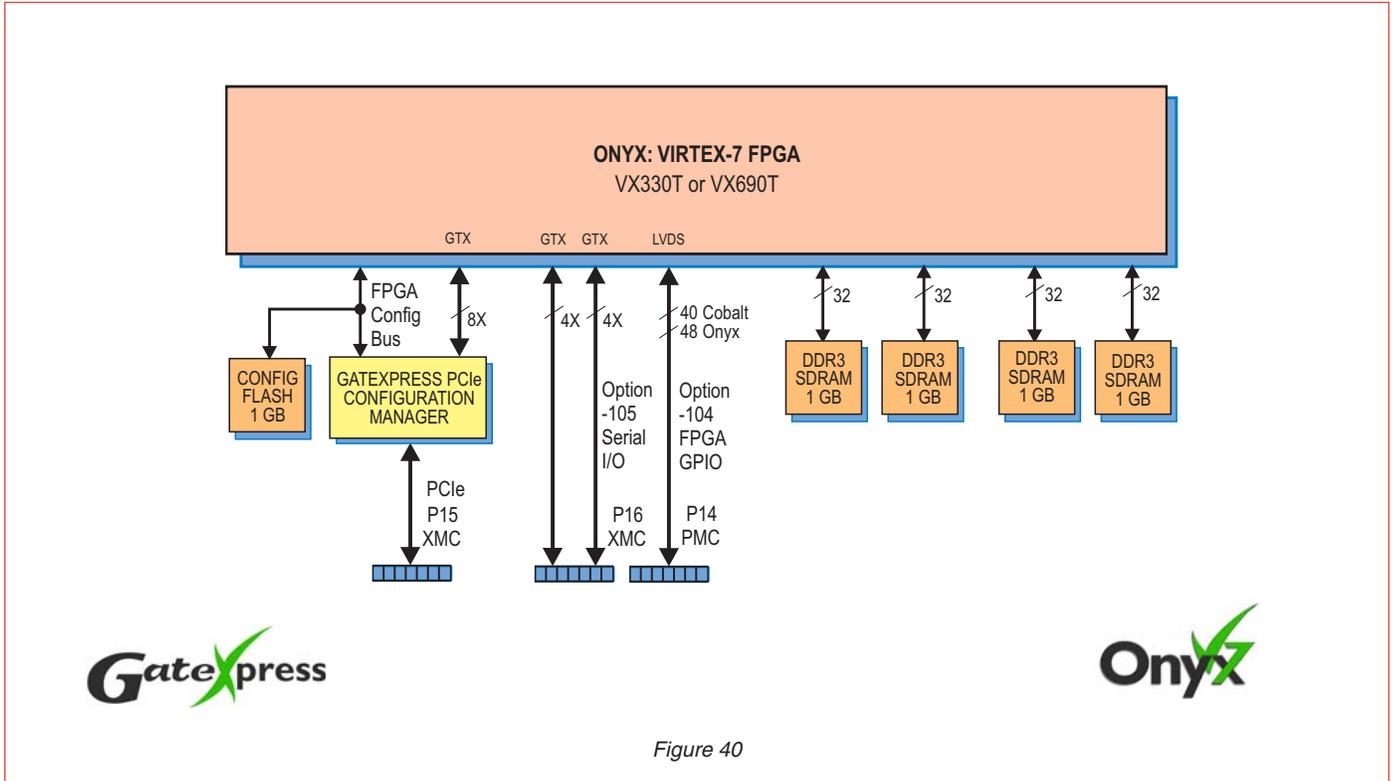
Figure 40

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

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Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores, Virtex-6 FPGA

Model 71621 XMC • Model 78621 PCIe • Model 53621 3U VPX • Model 56621 AMC
Model 72621 6U cPCI • Model 73621 3U cPCI • Model 74621 6U cPCI
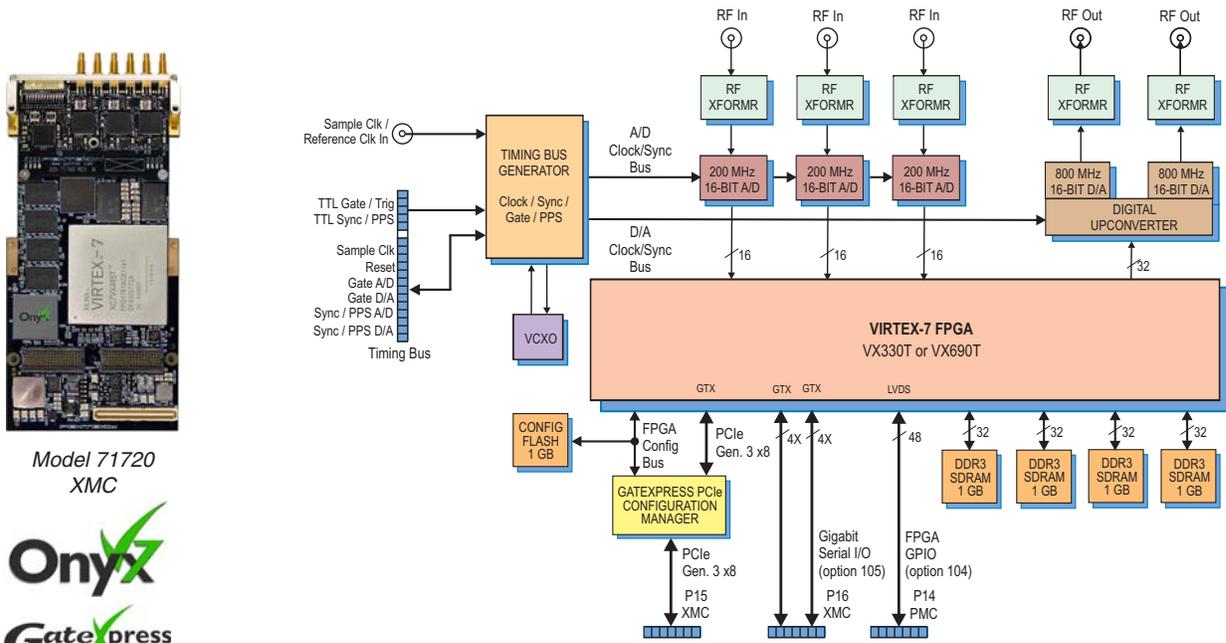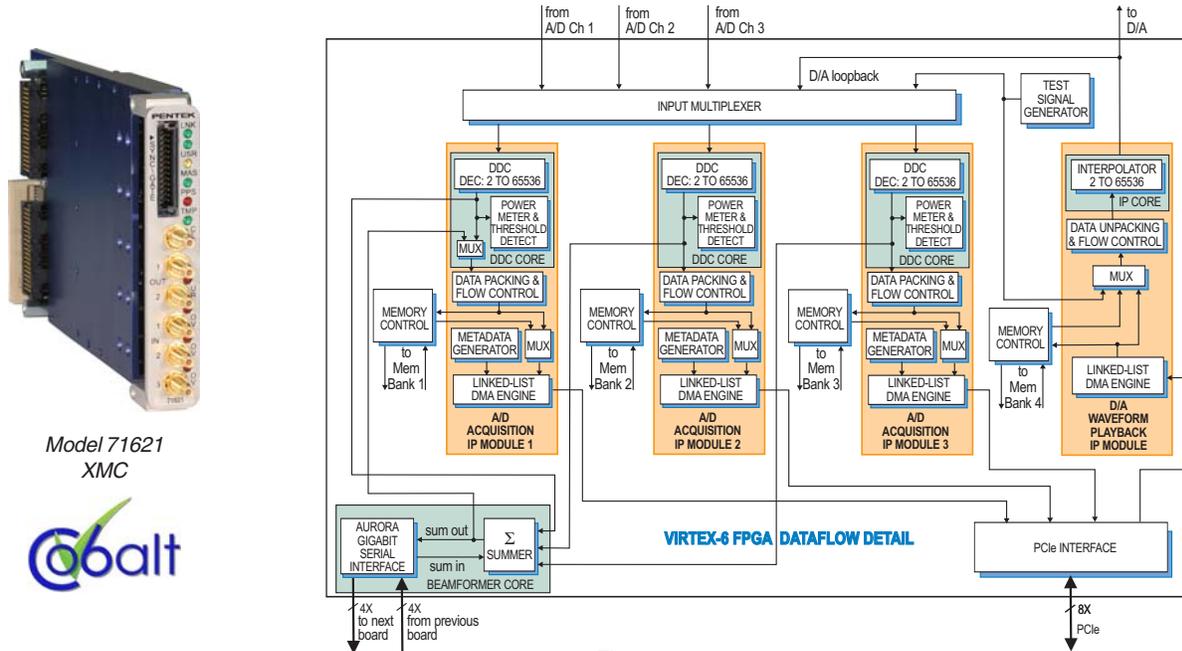

Model 71621 XMC

Figure 41

Model 71621 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71620 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71621 factory-installed functions include three A/D acquisition and one D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 71621 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Versions of the 71621 are also available as a PCIe half-length board (Model 78621), 3U VPX (Model 53621), AMC (Model 56621), 6U cPCI (Models 72621 and 74621 with dual density), and 3U cPCI (Model 73621).

1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA

Model 78630 PCIe • Model 71630 XMC • Model 53630 3U VPX • Model 56630 XMC
### Model 72630 6U cPCI • Model 73630 3U cPCI • Model 74630 6U cPCI
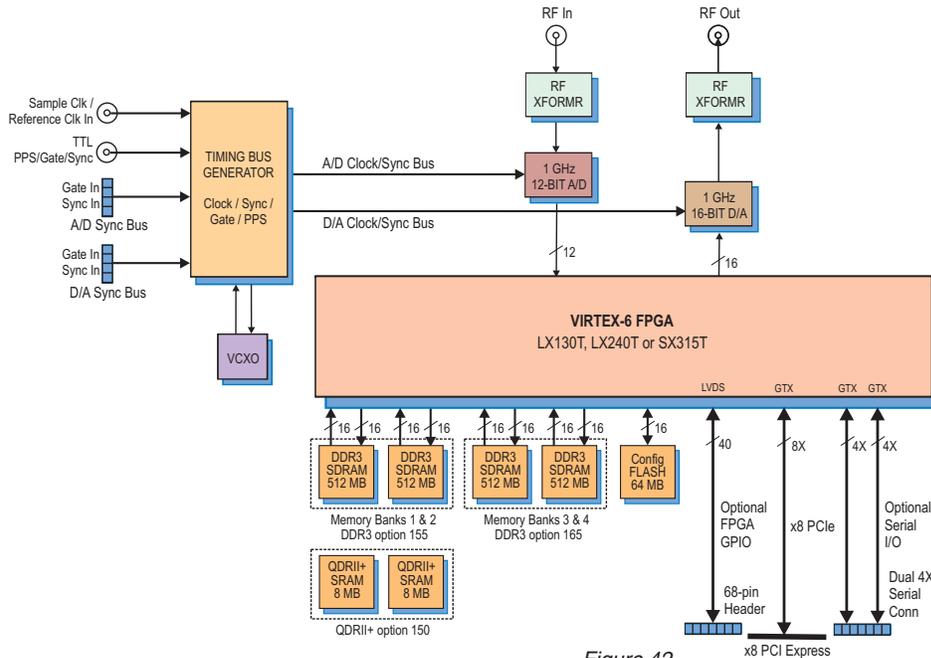
Figure 42

*Model 78630
x8 PCIe*

Model 78630 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes 1 GHz, 12-bit A/D, 1 GHz, 16-bit D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general purpose and gigabit serial card connectors for application-specific I/O protocols.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 78630's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 78630 are also available as an XMC module (Model 71630), 3U VPX (Model 53630), AMC (Model 56630), 6U cPCI (Models 72630 and 74630 with dual density), and 3U cPCI (Model 73630).

Products

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA

Model 72640 6U cPCI • Model 73640 3U cPCI • Model 74640 6U cPCI
Model 71640 XMC • Model 78640 PCIe • Model 53640 3U VPX • Model 56640 AMC
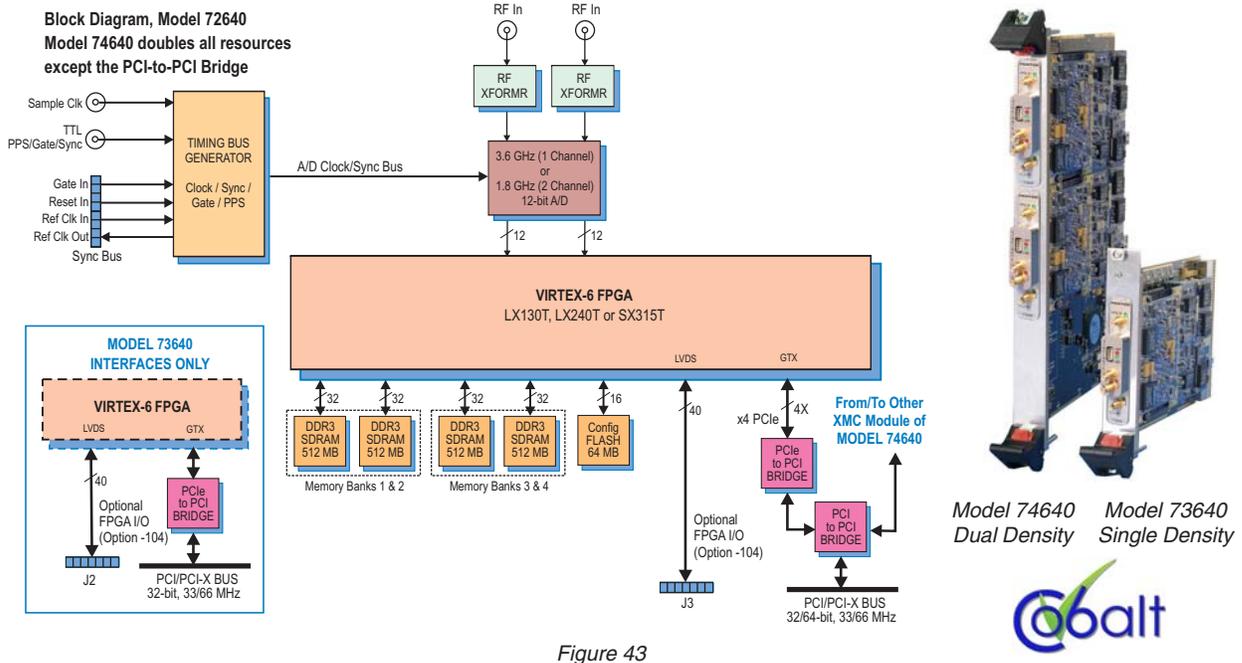
Figure 43

Models 72640, 73640 and 74640 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a cPCI carrier board. These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP

modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz. The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm.

Model 72640 is a 6U cPCI board, while Model 73640 is a 3U cPCI board; Model 74640 is a dual density 6U cPCI board. Also available is an XMC module (Model 71640), PCIe half-length board (Model 78640), 3U VPX (Model 53640), and AMC (Model 56640).

Products

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Wideband DDC, Virtex-6 FPGA

Model 56641 AMC • Model 71641 XMC • Model 78641 PCIe • Model 53641 3U VPX
Model 72641 6U cPCI • Model 73641 3U cPCI • Model 74641 6U cPCI
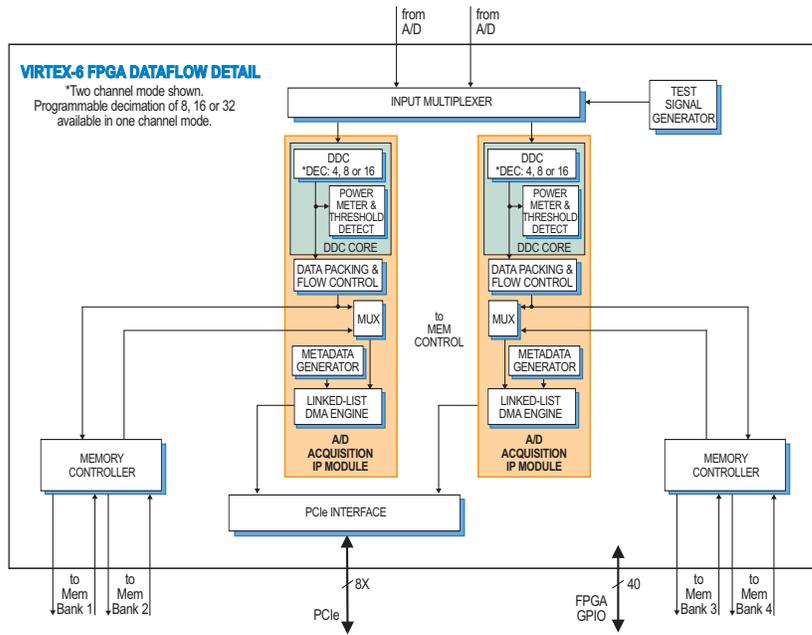
Model 56641 AMC

Figure 44

Model 56621 is a member of the Cobalt family of high performance AMC modules based on the Xilinx Virtex-6 FPGA. A very high-speed data converter based on the Model 56640 described in the previous page, it includes additional factory-installed IP cores to enhance the performance of the 56640 and address the requirements of many applications.

The 56641 factory-installed functions include an A/D acquisition IP module. In addition, within the FPGA is a powerful factory-installed DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Versions of the 56641 are also available as an XMC module (Model 71641), PCIe half-length board (Model 78641), 3U VPX (Model 53641), 6U cPCI (Models 72641 and 74641 dual density), and 3U cPCI (Model 73641).

2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA

Model 53650 3U VPX • Model 71650 XMC • Model 78650 PCIe • Model 56650 AMC
Model 72650 6U cPCI • Model 73650 3U cPCI • Model 74650 6U cPCI

This Model is also available with 400 MHz, 14-bit A/Ds
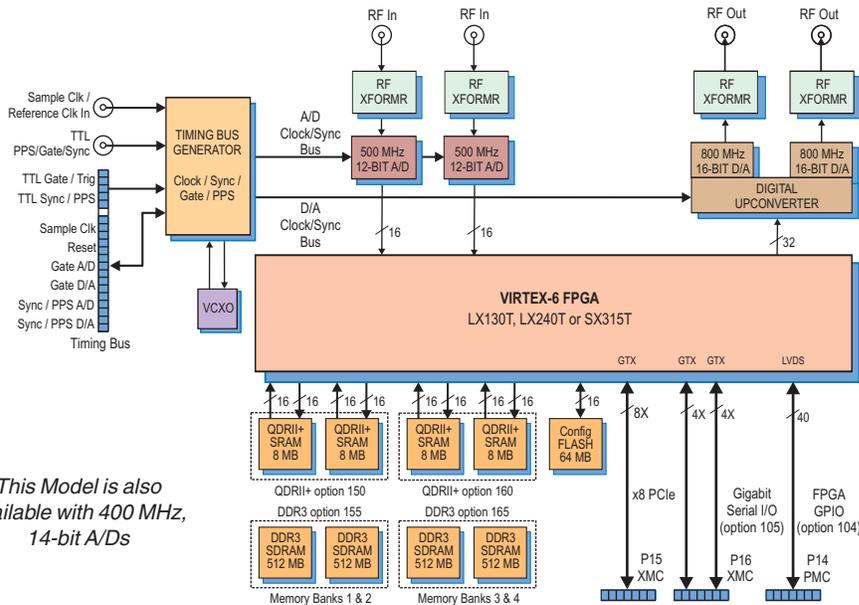
Model 53650 3U VPX
COTS and rugged

Figure 45

Model 53650 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 53650 includes two 500 MHz 12-bit A/Ds, one DUC, two 800 MHz 16-bit D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53650 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 53650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 53650 are also available as an XMC module (Model 71650), as a PCIe half-length board (Model 78650), AMC (Model 56650), 6U cPCI (Models 72650 and 74650 with dual density), and 3U cPCI (Model 73650).

2- or 4-Channel 500 MHz A/D, with DDCs, DUCs, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA

Model 72651 6U cPCI • Model 73651 3U cPCI • Model 74651 6U cPCI
Model 53651 3U VPX • Model 71651 XMC • Model 78651 PCIe • Model 56651 AMC
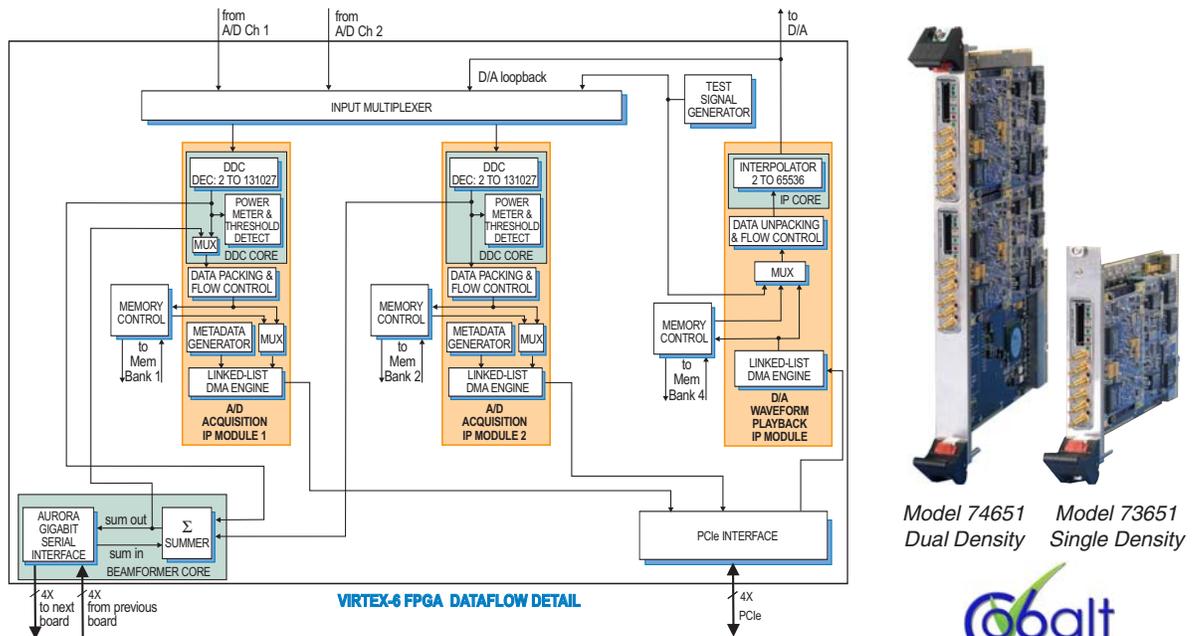
Figure 46

Models 72651, 73651 and 74651 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71651 XMC modules mounted on a cPCI carrier board. These models include two or four A/Ds, two or four multiband DDCs, one ot two DUCs, two or four D/As and three or six banks of memory.

These models feature two or four A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP module in loopback mode.

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two or four different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

Model 72651 is a 6U cPCI board, while Model 73651 is a 3U cPCI board; Model 74651 is a dual density 6U cPCI board. Also available is an XMC module (Model 71651), PCIe half-length board (Model 78651), 3U VPX (Model 53651), and AMC (Model 56651).

Products

4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA

Model 71660 XMC • Model 78660 PCIe • Model 53660 3U VPX • Model 56660 AMC
Model 72660 6U cPCI • Model 73660 3U cPCI • Model 74660 6U cPCI
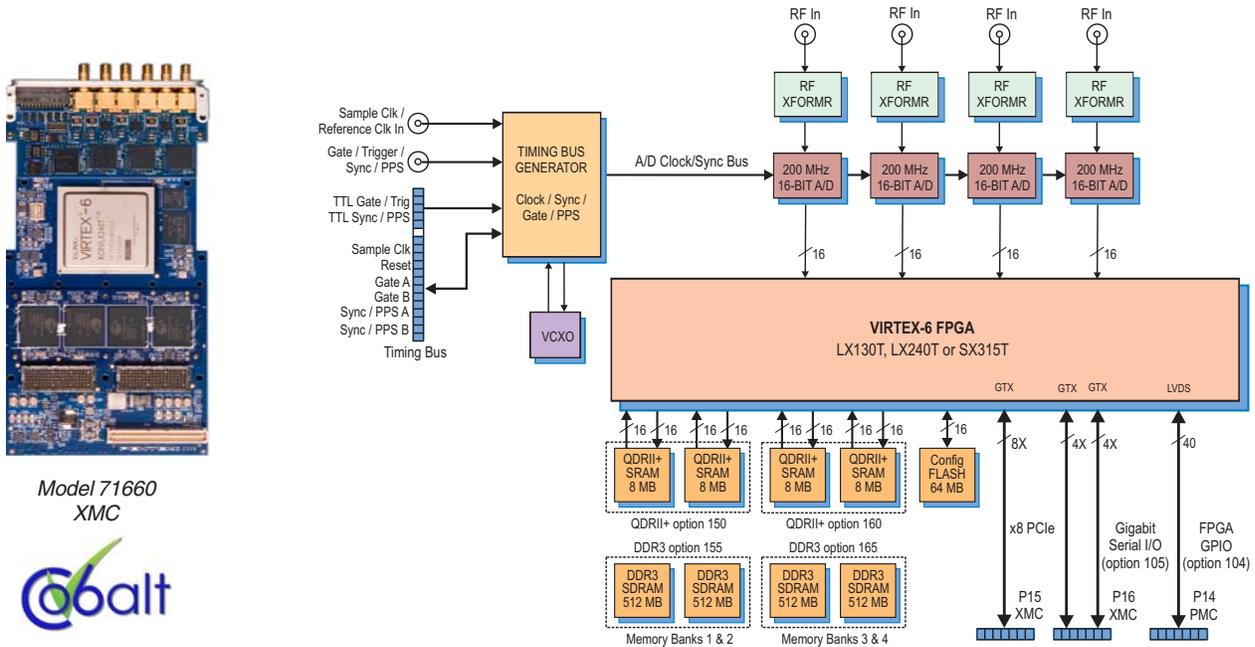
Model 71660 XMC

Figure 47

Model 71660 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four 200 MHz, 16-bit A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O .

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 71660 are also available as a PCIe half-length board (Model 78660), 3U VPX (Model 53660), AMC (Model 56660), 6U cPCI (Models 72660 and 74660 with dual density), and 3U cPCI (Model 73660).

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Products

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA

Model 71760 XMC • Model 78760 PCIe • Model 53760 3U VPX • Model 56760 AMC
### Model 72760 6U cPCI • Model 73760 3U cPCI • Model 74760 6U cPCI

Model 71760 XMC

Figure 48

Model 71760 is a member of the Onyx family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71760 includes general purpose and gigabit serial connectors for application-specific I/O.

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

The 71760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Versions of the 71760 are also available as a PCIe half-length board (Model 78760), 3U VPX (Model 53760), AMC (Model 56760), 6U cPCI (Models 72760 and 74760 dual density), and 3U cPCI (Model 73760).

Please go to page 29 for information about GateXpress.

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Products

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA

Model 71661 XMC • Model 78661 PCIe • Model 53661 3U VPX • Model 56661 AMC
Model 72661 6U cPCI • Model 73661 3U cPCI • Model 74661 6U cPCI
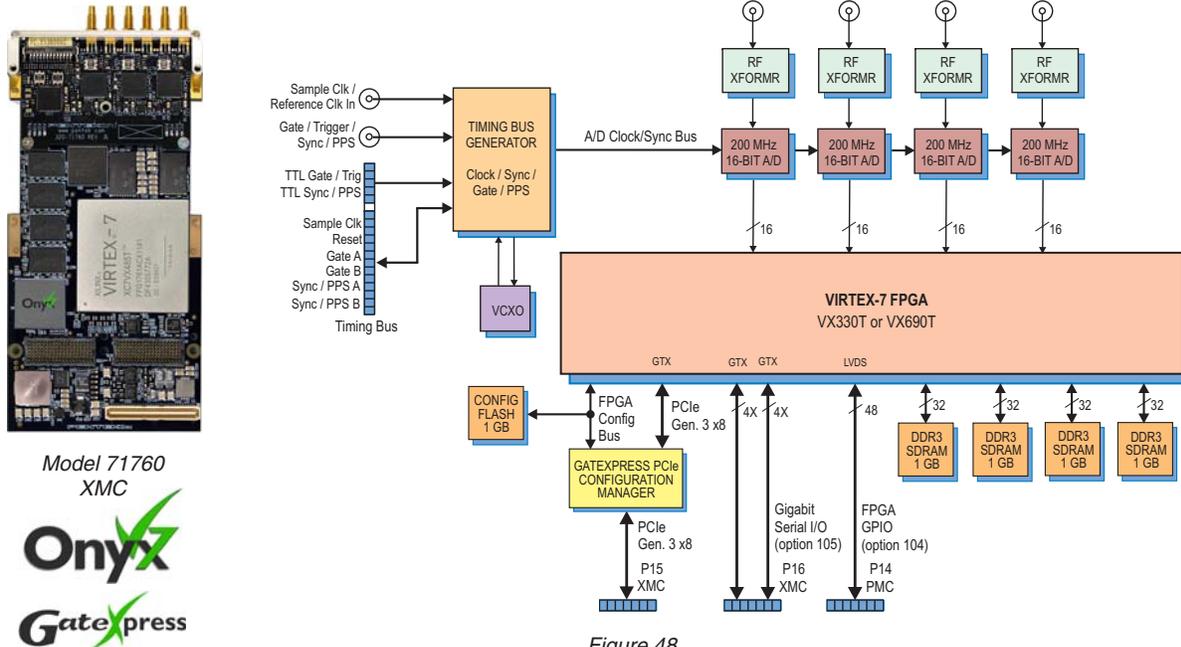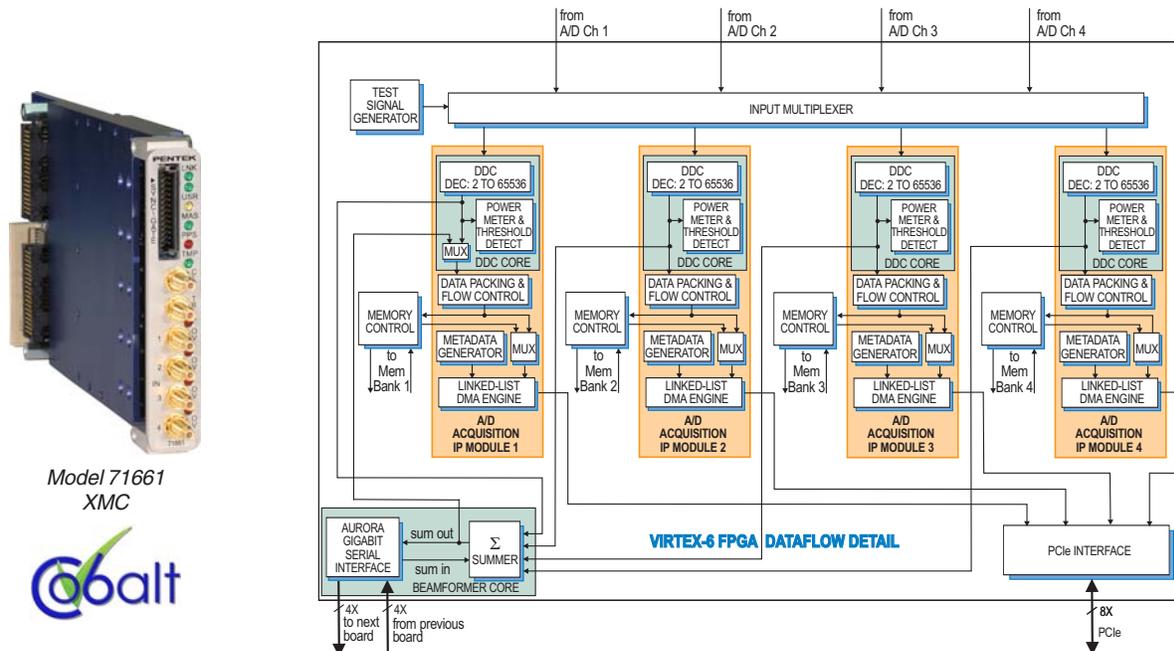
Model 71661 XMC

Figure 49

Model 71661 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71660 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71661 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decima-

tions can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 71661 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

For larger systems, multiple 71661's can be chained together via the built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector.

Versions of the 71661 are also available as a PCIe half-length board (Model 78661), 3U VPX (Model 53661), AMC (Model 56661), 6U cPCI (Models 72661 and 74661 with dual density), and 3U cPCI (Model 73661).

Products

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA

Model 78662 PCIe • Model 71662 XMC • Model 53662 3U VPX • Model 56662 AMC
Model 72662 6U cPCI • Model 73662 3U cPCI • Model 74662 6U cPCI
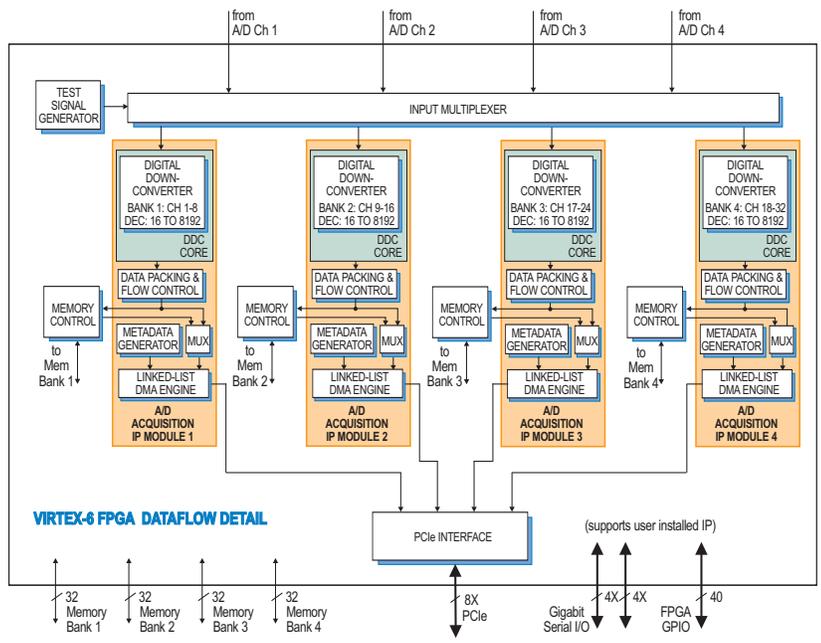
Model 78662 x8 PCIe

Figure 50

Model 78662 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. Based on the Model 71660 presented previously, this four-channel, high-speed data converter with programmable DDCs is suitable for connection to HF or IF ports of a communications or radar system.

The 78662 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, voltage and temperature monitoring, and a PCIe interface complete the factory-installed functions.

Each of the 32 DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting ranging from 16 to 8192 programmable in steps

of eight. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Multiple 78662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Versions of the 78662 are also available as an XMC module (Model 71662), 3U VPX (Model 53662), AMC (Model 56662), 6U cPCI (Models 72662 and 74662 with dual density), and 3U cPCI (Model 73662).

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Products

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA

Model 56670 AMC • Model 71670 XMC • Model 78670 PCIe • Model 53670 3U VPX
### Model 72670 6U cPCI • Model 73670 3U cPCI • Model 74670 6U cPCI
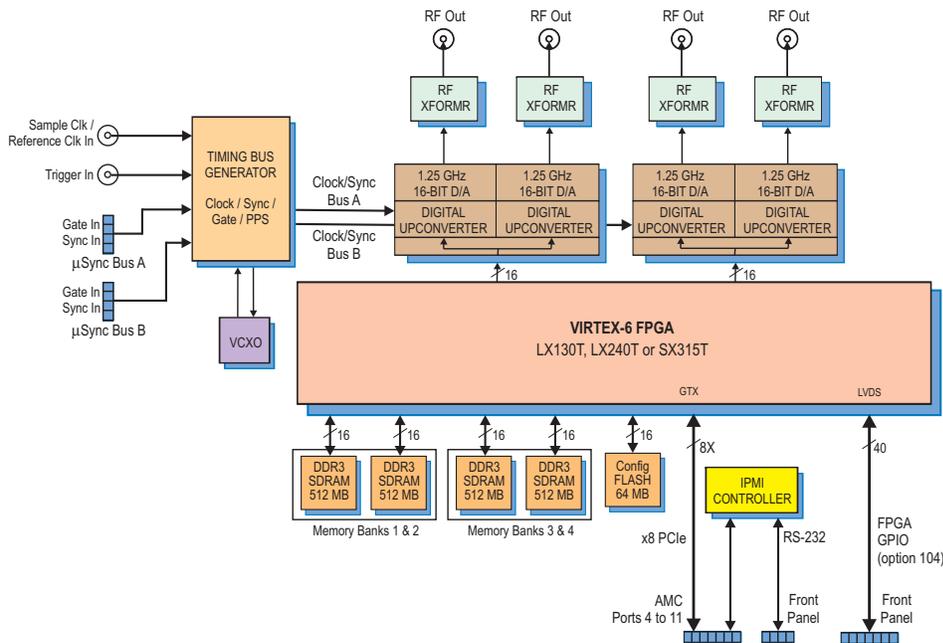
Figure 51

Model 56670 is a member of the Cobalt family of high performance AMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications. It includes four D/As, four digital upconverters and four banks of memory.   In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56670 includes a front panel general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

The Model 56670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Versions of the 56670 are also available as an XMC module (Model 71670), PCIe half-length board (Model 78670), 3U VPX (Model 53670), 6U cPCI (Models 72670 and 74670 dual density), and 3U cPCI (Model 73670).

Products

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation, Virtex-6 FPGA

Model 71671 XMC • Model 78671 PCIe • Model 53671 3U VPX • Model 56671 AMC
Model 72671 6U cPCI • Model 73671 3U cPCI • Model 74671 6U cPCI

Model 71671 XMC

Figure 52

Model 71671 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71670 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71670 and address the requirements of many applications.

The Model 56671 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user

selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x.

In addition to the DAC3484, the 71671 features an FPGA-based interpolation engine which adds two additonal interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems.

Versions of the 71671 are also available as a PCIe half-length board (Model 78671), 3U VPX (Model 53671), AMC (Model 56671), 6U cPCI (Models 72671 and 74671 with dual density), and 3U cPCI (Model 73671).

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Products

L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA

Model 53690 3U VPX • Model 71690 XMC • Model 78690 PCIe • Model 56690 AMC
Model 72690 6U cPCI • Model 73690 3U cPCI • Model 74690 6U cPCI
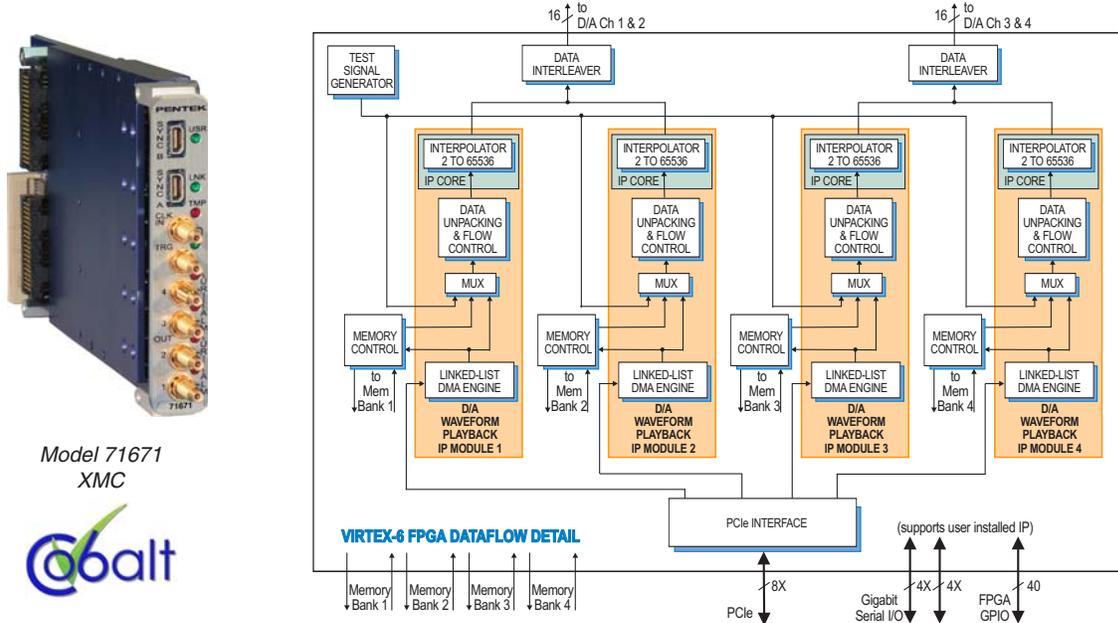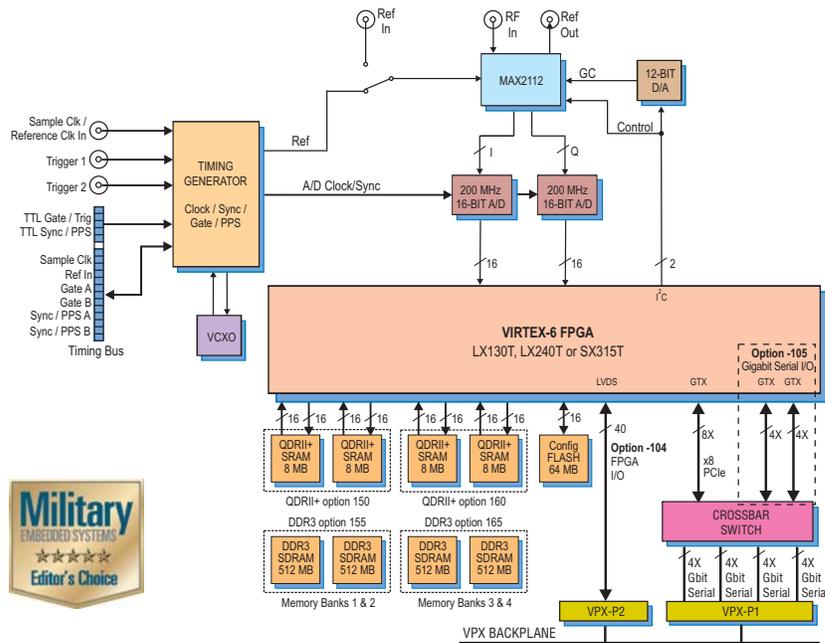

*Model 53690 3U VPX
COTS and rugged*

Figure 53

Model 53690 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. The Model 53690 includes an L-Band RF tuner, two 200 MHz, 16-bit A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the

board's analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

A front panel connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB. A Maxim MAX2112 tuner directly converts these signals to baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA (low-noise amplifier), a PLL synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters and variable-gain baseband amplifiers.

Versions of the 53690 are also available as an XMC module (Model 71690), as a PCIe half-length board (Model 78690), AMC (Model56690), 6U cPCI (Models 72690 and 74690 with dual density), and 3U cPCI (Model 73690).

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Products

2.2 GHz Clock, Sync and Gate Distribution Board

Model 6890 - VME

Figure 54

Model 6890
VME

Model 6890 Clock, Sync and Gate Distribution Board synchronizes multiple Pentek I/O boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications. Up to eight boards can be synchronized using the 6890, each receiving a common clock of up to 2.2 GHz along with timing signals that can be used for synchronizing, triggering and gating functions.

Clock signals are applied from an external source such as a high performance sine wave generator. Gate and sync signals can come from an external source, or from one supported board set to act as the master.

The 6890 accepts clock input at +10 dBm to +14 dBm with a frequency range from 800 MHz to 2.2 GHz and uses a 1:2 power splitter to distribute the clock. The first output of this power splitter sends the clock signal to a 1:8 splitter for distribution to up to eight boards using SMA connectors. The second output of the 1:2 power

splitter feeds a 1:2 buffer which distributes the clock signal to both the gate and synchronization circuits.

The 6890 features separate inputs for gate/trigger and sync signals with user-selectable polarity. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable inputs allow the user to enable or disable these circuits using an external signal.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer. A bank of eight MMCX connectors at the output of each buffer delivers signals to up to eight boards.

A 2:1 multiplexer in each circuit allows the gate/trigger and sync signals to be registered with the input clock signal before output, if desired.

Sets of input and output cables for two to eight boards are available from Pentek.

Products

System Synchronizer and Distribution Board

Model 6891 - VME

Figure 55
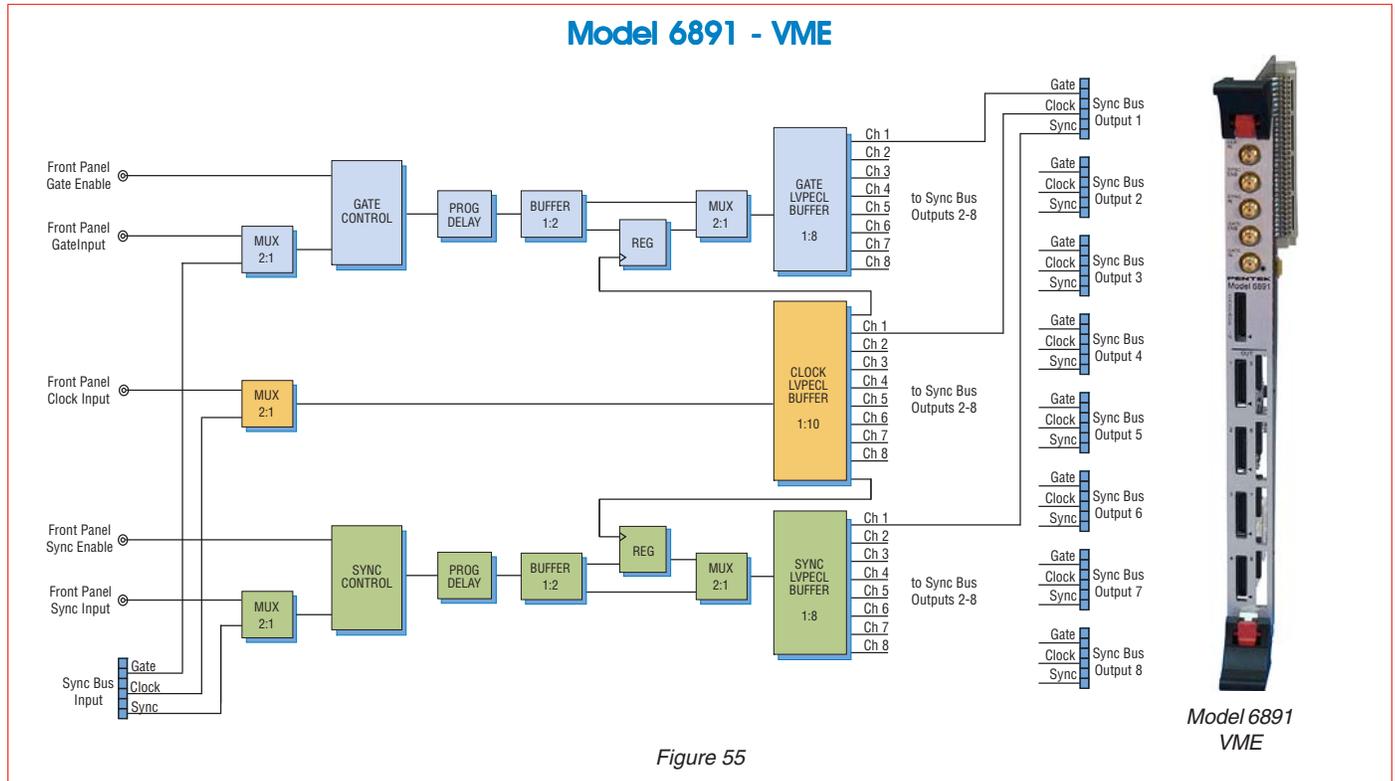
*Model 6891
VME*
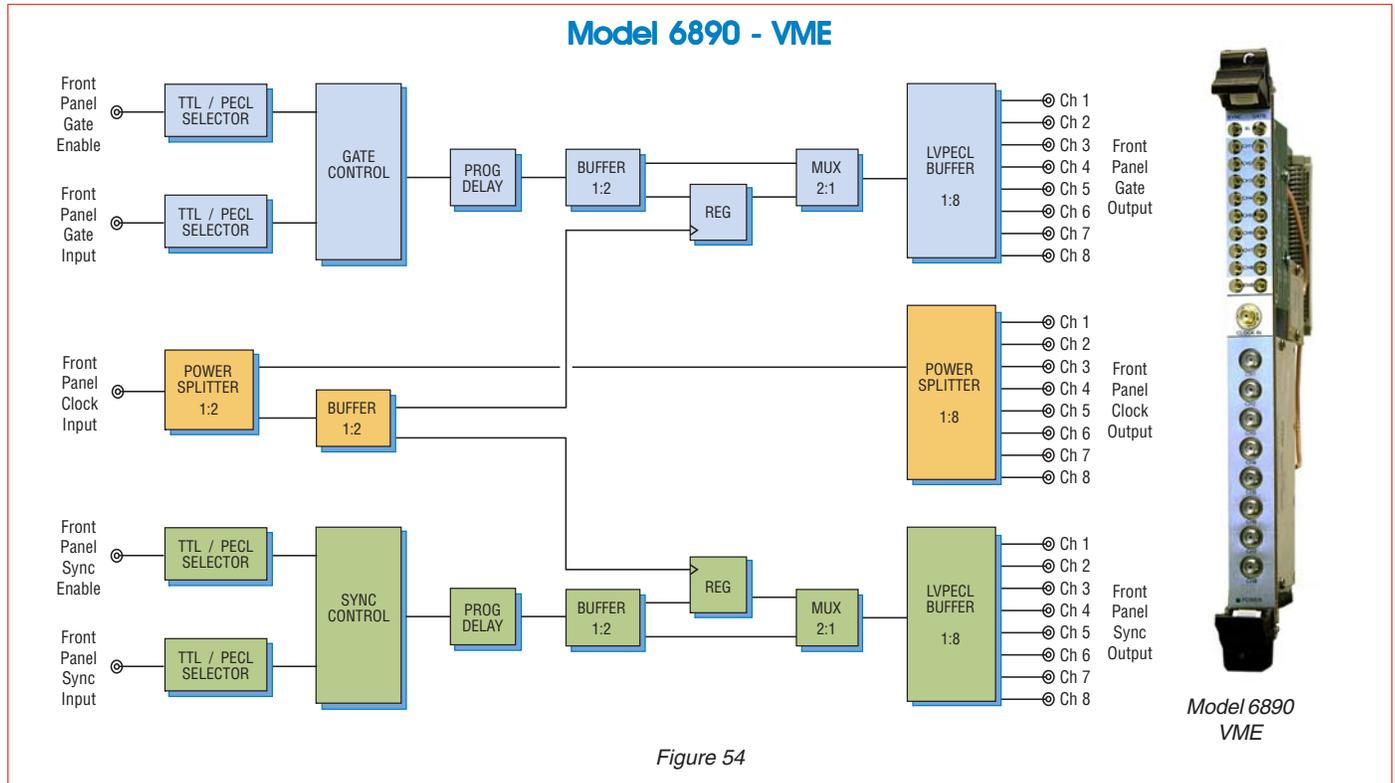
Model 6891 System Synchronizer and Distribution Board synchronizes multiple Pentek I/O modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight modules can be synchronized using the 6891, each receiving a common clock up to 500 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 6891's can be linked together to provide synchronization for up to 64 I/O modules producing systems with up to 256 channels.

Model 6891 accepts three TTL input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Two additional inputs are provided for separate gate and sync enable signals.

Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. Alternately, a Sync Bus connector accepts LVPECL inputs from any compatible Pentek products to drive the clock, sync and gate/trigger signals.

The 6891 provides eight front panel Sync Bus output connectors, compatible with a wide range of Pentek I/O modules. The Sync Bus is distributed through ribbon cables, simplifying system design. The 6891 accepts clock input at +10 dBm to +14 dBm with a frequency range from 1 kHz to 800 MHz. This clock is used to register all sync and gate/trigger signals as well as providing a sample clock to all connected I/O modules.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer for output through the Sync Bus connectors.

Multifrequency Clock Synthesizer

Model 7190 PMC • Model 7290 6U cPCI • Model 7390 3U cPCI • Model 7690 PCI
Model 7790 Full-length PCIe • Model 7890 Half-length PCIe • Model 5390 3U VPX

Model 7190 PMC

Figure 56

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs and can be phase-locked to an external reference signal.

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 MHz and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7190 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7190's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7190 are also available as a PCIe full-length board (Models 7790 and 7790D dual density), PCIe half-length board (Model 7890), 3U VPX board (Model 5390), PCI board (Model 7690), 6U cPCI (Models 7290 and 7290D dual density), or 3U cPCI (Model 7390).

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Programmable Multifrequency Clock Synthesizer

Model 7191 PMC • Model 7291 6U cPCI • Model 7391 3U cPCI • Model 7691 PCI
Model 7791 Full-length PCIe • Model 7891 Half-length PCIe • Model 5391 3U VPX
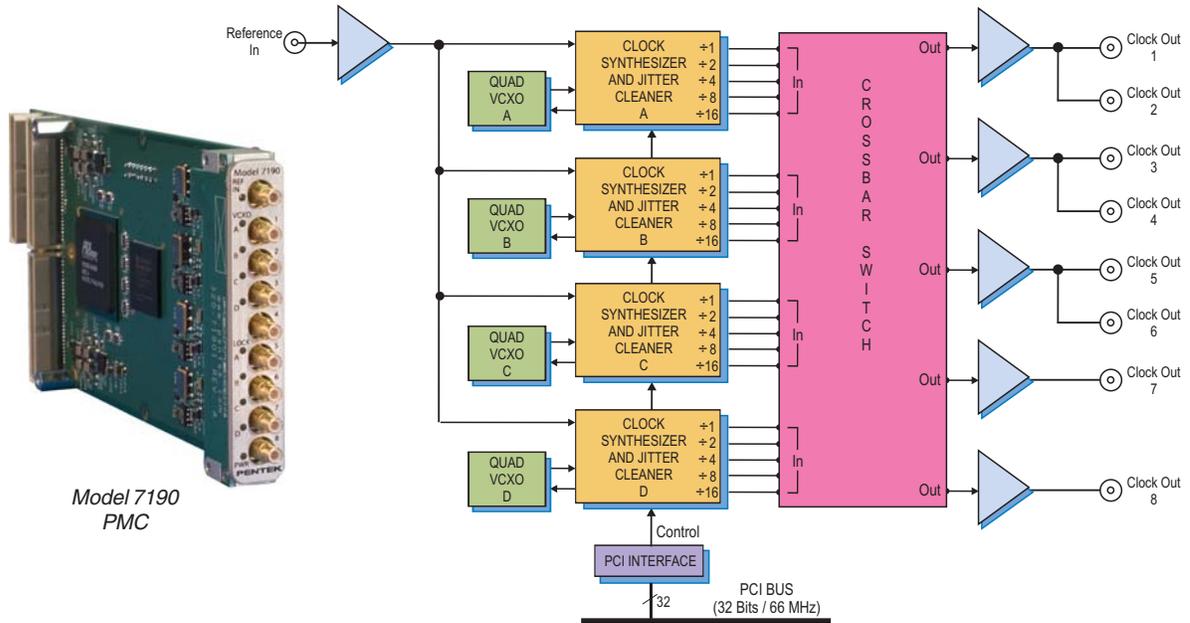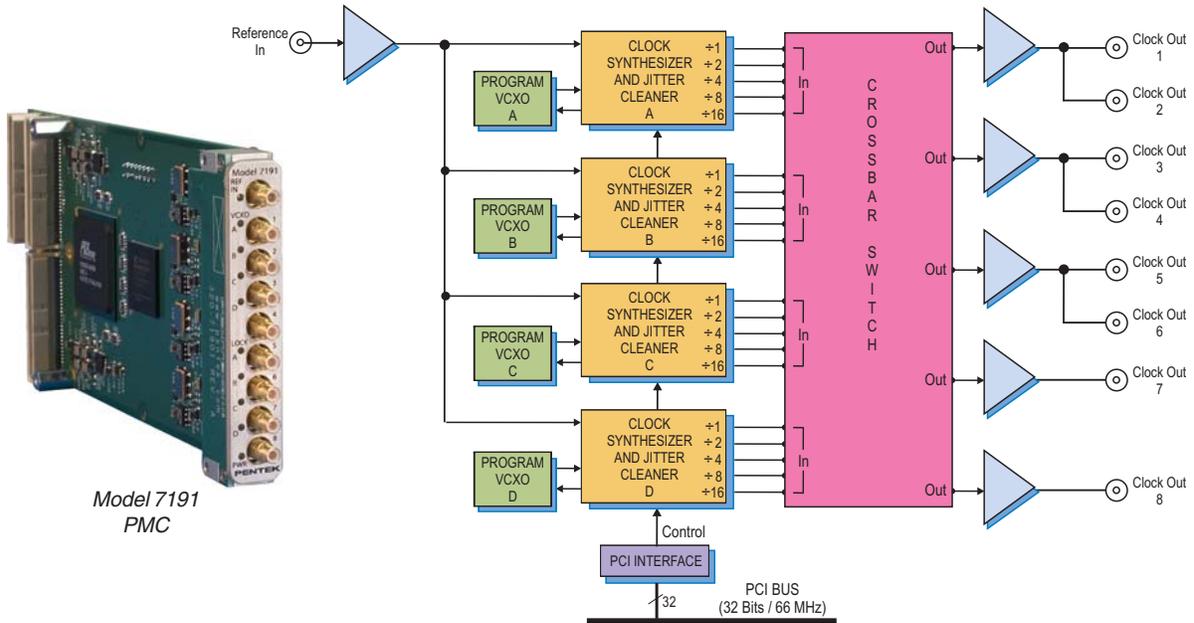

Model 7191
PMC

Figure 57

Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from programmable VCXOs and can be phase-locked to an external reference signal.

The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 MHz and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7191 are also available as a PCIe full-length board (Models 7791 and 7791D dual density), PCIe half-length board (Model 7891), 3U VPX board (Model 5391), PCI board (Model 7691), 6U cPCI (Models 7291 and 7291D dual density), or 3U cPCI (Model 7391).

Products

High-Speed Synchronizer and Distribution Board

Model 7192 PMC/XMC • Model 7892 Half-length PCIe • Model 5393 3U VPX
Model 7292 6U cPCI • Model 7392 3U cPCI • Model 7492 6U cPCI

*Model 7192
PMC/XMC*

Figure 58

The Model 7192 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to four modules can be synchronized using the 7192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 7192 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

The 7192 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx modules. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design. The 7192 features a calibration output specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 7192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 7192 will also support high-speed models in the Onyx family as they become available.

Versions of the 7192 are also available as a PCIe half-length board (Model 7892), 3U VPX (Model 5392), 6U cPCI (Models 7292 and 7492 dual density), and 3U cPCI (Model 7392).

Products

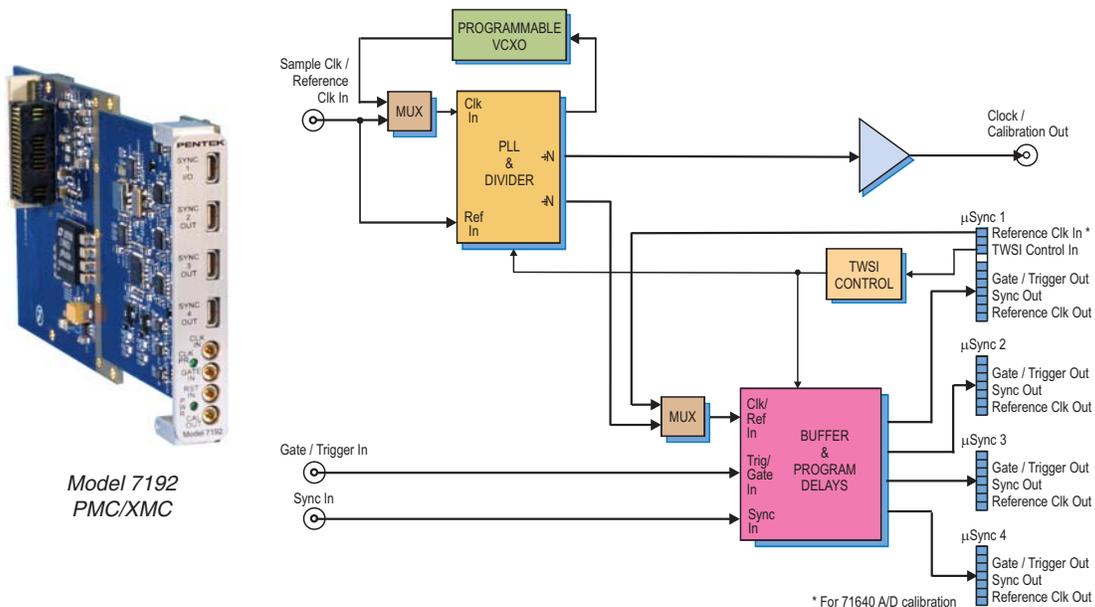## System Synchronizer and Distribution Board

Model 7893 - Half-length PCIe

Figure 59
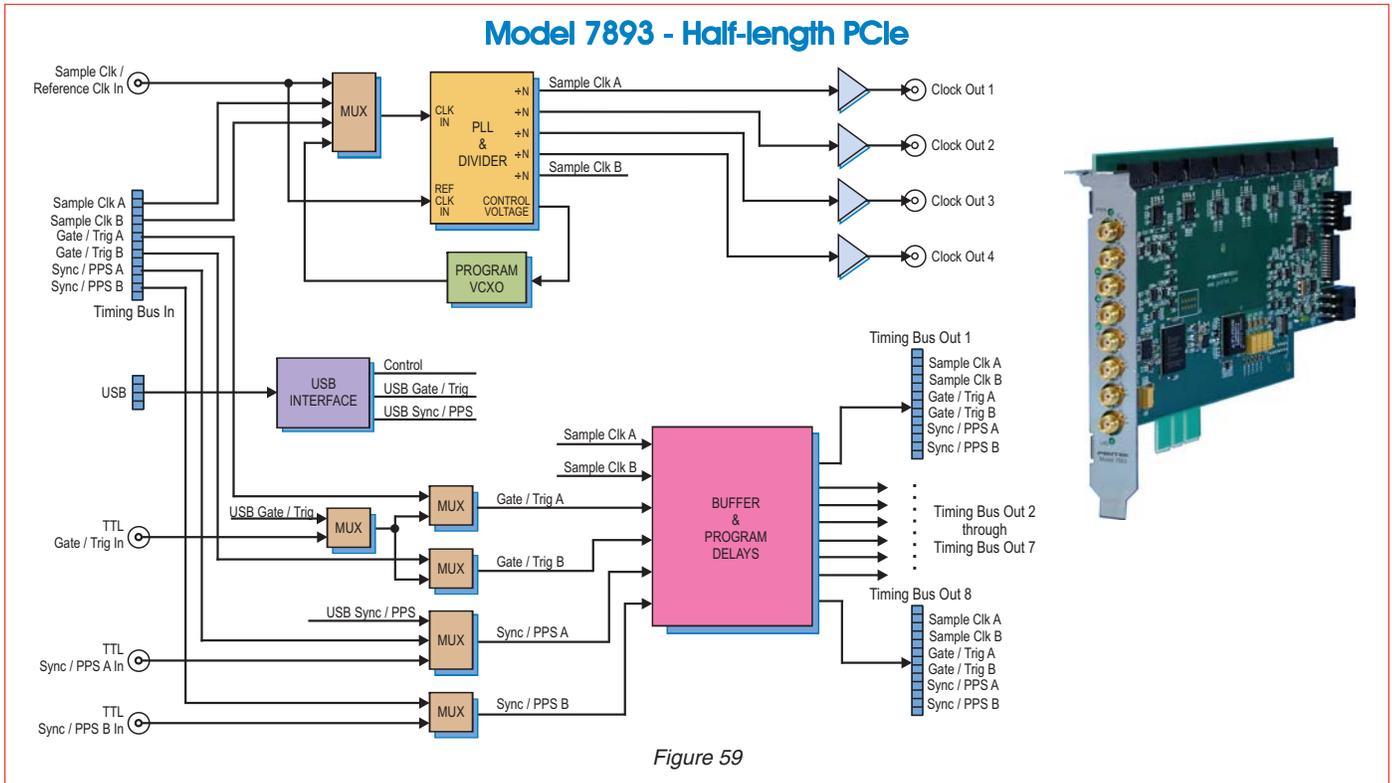
Model 7893 System Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt and Onyx boards within a system. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight boards can be synchronized using the 7893, each receiving a common clock up to 800 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 7893s can be linked together to provide synchronization for up to 64 Cobalt or Onyx boards.

The Model 7893 provides four front panel SMA connectors to accept LVTTL input signals from external sources: two for Sync/PPS and one for Gate/Trigger. In addition to the synchronization signals, a front panel SMA connector accepts sample clocks up to 800 MHz or, in an alternate mode, accepts a 10 MHz reference clock to lock an on-board VCXO sample clock source.

The 7893 provides eight timing bus output connectors for distributing all needed timing and clock signals to the front panels of Cobalt and Onyx boards via ribbon cables. The 7893 locks the Gate/Trigger and Sync/PPS signals to the system's sample clock. The 7893 also provides four front panel SMA connectors for distributing sample clocks to other boards in the system.

The 7893 can accept a clock from either the front panel SMA connector or from the timing bus input connector. A programmable on-board VCXO clock generator can be locked to a user-supplied, 10 MHz reference.

The 7893 supports a wide range of products in the Cobalt family including the 78620 and 78621 three-channel A/D 200 MHz transceivers, the 78650 and 78651 two-channel A/D 500 MHz transceivers, the 78660, 78661 and 78662 four-channel 200 MHz A/Ds, and the 78690 L-Band RF Tuner. The 7893 also supports the Onyx 78760 four-channel 200 MHz A/D and will support all complementary models in the Onyx family as they become available.

Products

Clock and Sync Generator for I/O Modules

Model 9190 - Rack-mount

Model 9190

Figure 60
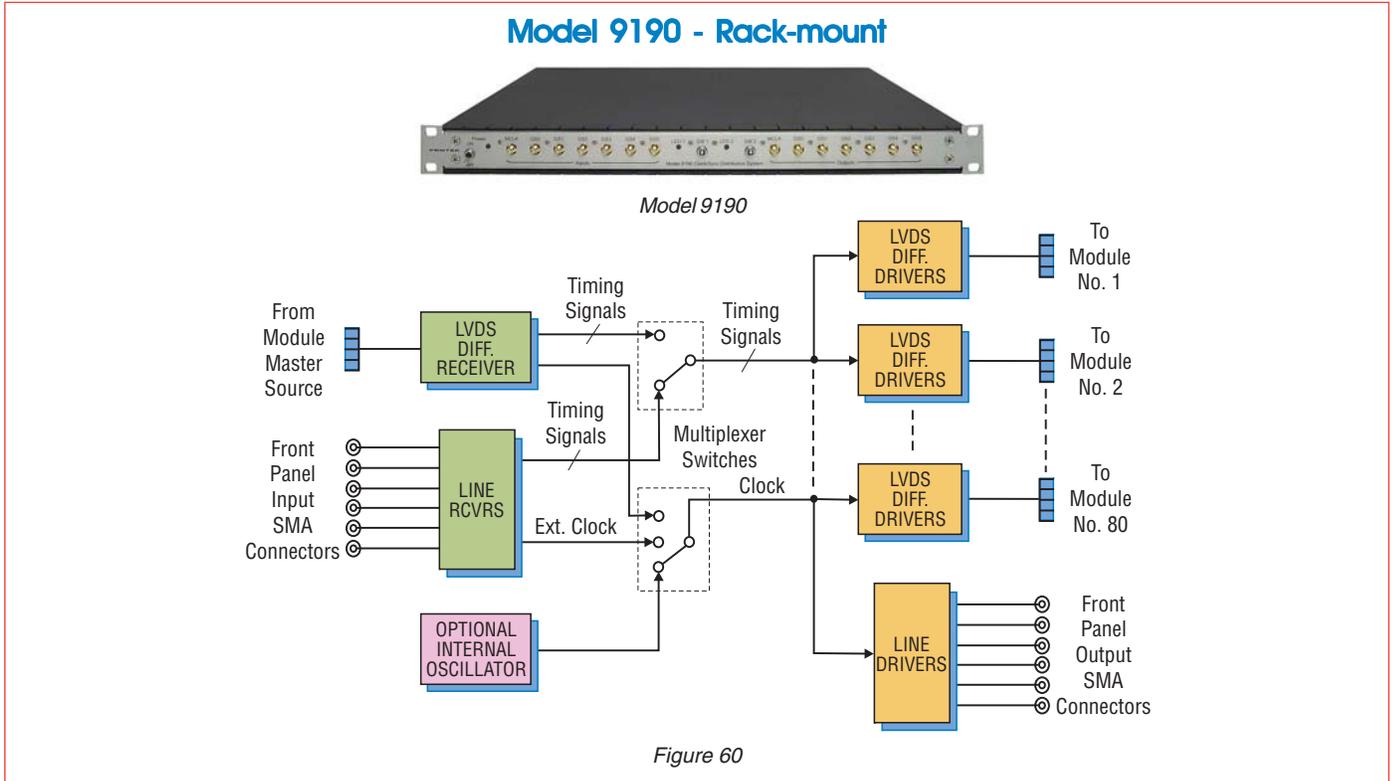
Model 9190 Clock and Sync Generator synchronizes multiple Pentek I/O modules within a system to provide synchronous sampling and timing for a wide range of high-speed, multichannel data acquisition, DSP and software radio applications. Up to 80 I/O modules can be driven from the Model 9190, each receiving a common clock and up to five different timing signals which can be used for synchronizing, triggering and gating functions.

Clock and timing signals can come from six front panel SMA user inputs or from one I/O module set to act as the timing signal master. (In this case, the master I/O module will not be synchronous with the slave modules due to delays through the 9190.) Alternately, the master clock can come from a socketed, user-replaceable crystal oscillator within the Model 9190.

Buffered versions of the clock and five timing signals are available as outputs on the 9190's front panel SMA connectors.

Model 9190 is housed in a line-powered, 1.75 in. high metal chassis suitable for mounting in a standard 19 in. equipment rack, either above or below the cage holding the I/O modules.

Separate cable assemblies extend from openings in the front panel of the 9190 to the front panel clock and sync connectors of each I/O module. Mounted between two standard rack-mount card cages, Model 9190 can drive a maximum of 80 clock and sync cables, 40 to the card cage above and 40 to the card cage below. Fewer cables may be installed for smaller systems.

Products

High-Speed System Synchronizer Unit

Model 9192 - Rack-mount
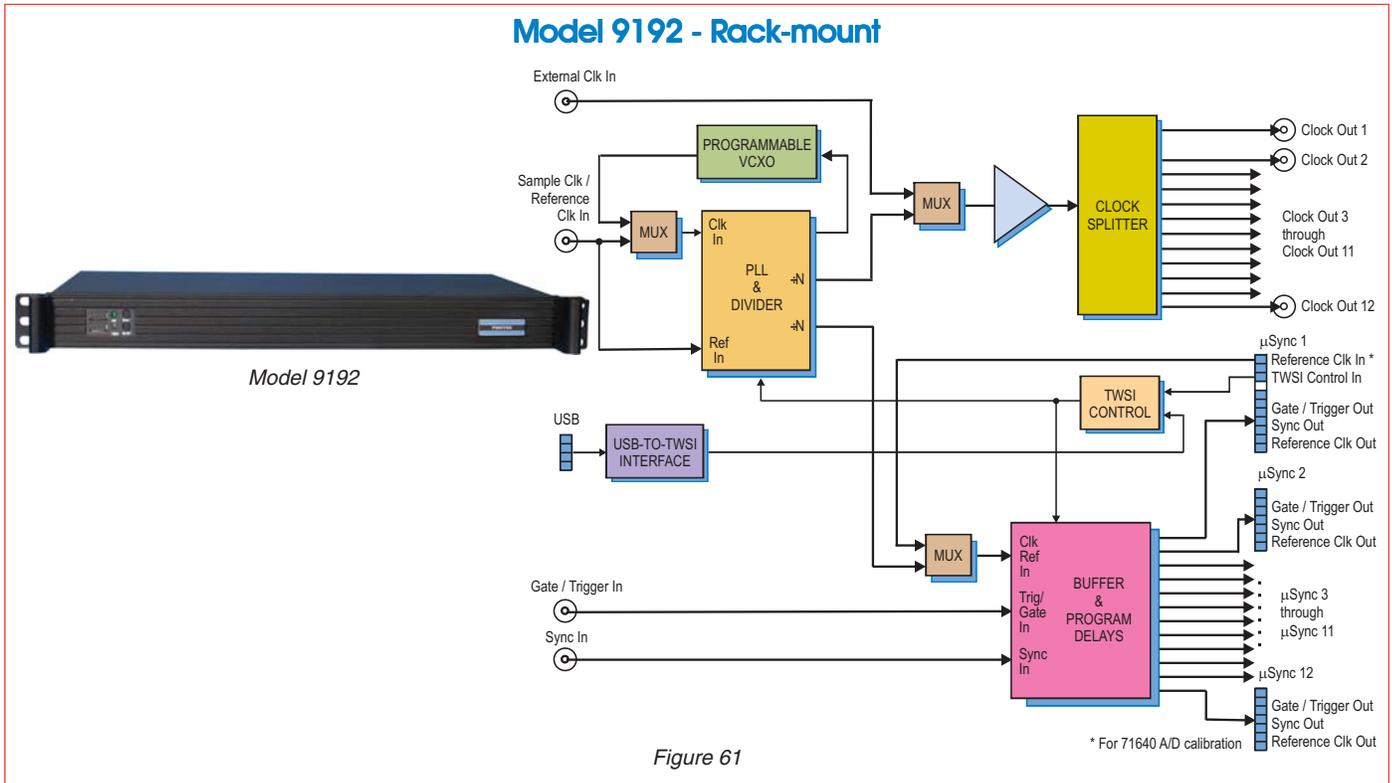
Figure 61

Model 9192 Rack-mount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to twelve boards can be synchronized using the 9192, each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

The 9192 provides four rear panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

The 9192 features twelve calibration outputs specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 9192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 9192 will also support high-speed models in the Onyx family as they become available.

Products

Eight-Channel RF/IF, 200 MS/sec Rackmount Recorder

Model RTS 2706

Model RTS 2706 COTS

Model RTS 2706 Rugged

Figure 62

The Talon® RTS 2706 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2706 uses 16-bit, 200 MHz A/D converters and provides sustained recording rates up to 2.0 GB/sec in four-channel configuration.

The RTS 2706 uses Pentek's high-powered Virtex-6-based Cobalt modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate and DUC interpolation are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals.

Included with this system is Pentek's SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.

Built on a Windows® 7 Professional workstation with high performance Intel® Core™ i7 processor, the RTS 2706 allows the user to install post-processing and analysis tools to operate on the recorded data. The instrument records data to the native NTFS file system, providing immediate access to the data.

The RTS 2706 is configured in a 4U 19" rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

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Products

Four-Channel RF/IF, 500 MS/sec Rackmount Recorder

Model RTS 2707

Channels In → 500 MHz 12-bit A/D or 400 MHz 14-bit A/D Up to 4 Channels → DIGITAL DOWN-CONVERTER DEC: 2 to 64K

Channels Out ← 800 MHz 16-bit D/A Up to 4 Channels ← DIGITAL UP-CONVERTER INT: 2 to 64K

INTEL PROCESSOR
SYSTEM DRIVE
DDR SDRAM
HOST PROCESSOR RUNNING SYSTEMFLOW

Gigabit Ethernet
USB 2.0
PS/2 Keyboard
PS/2 Mouse
Video Output
GPS Antenna (Optional)

DATA DRIVES
DATA DRIVES
DATA DRIVES
DATA DRIVES
RAID DATA STORE

MODEL RTS 2707

TALON RTS COMMERCIAL RECORDER
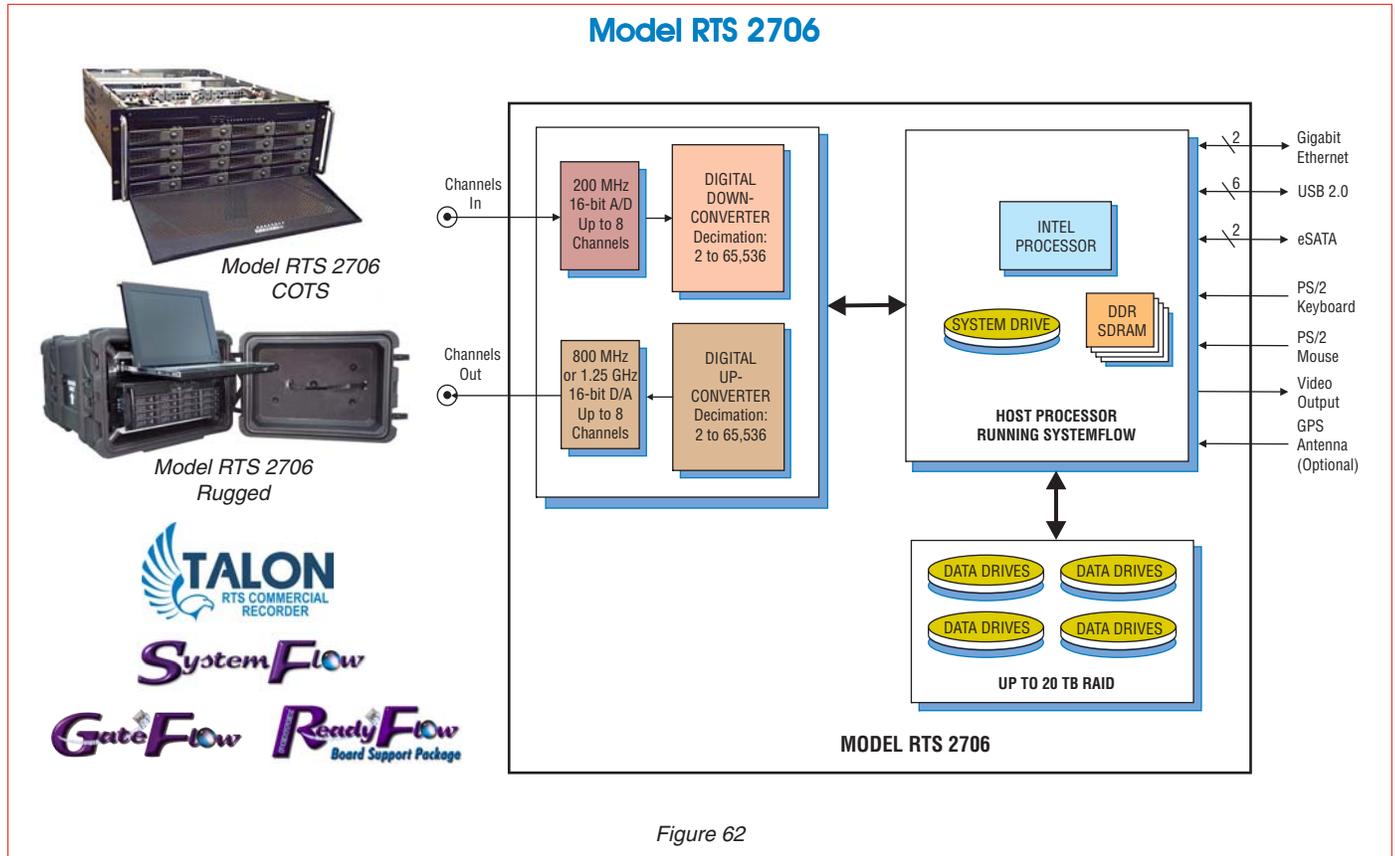SystemFlow
GateFlow
ReadyFlow Board Support Package
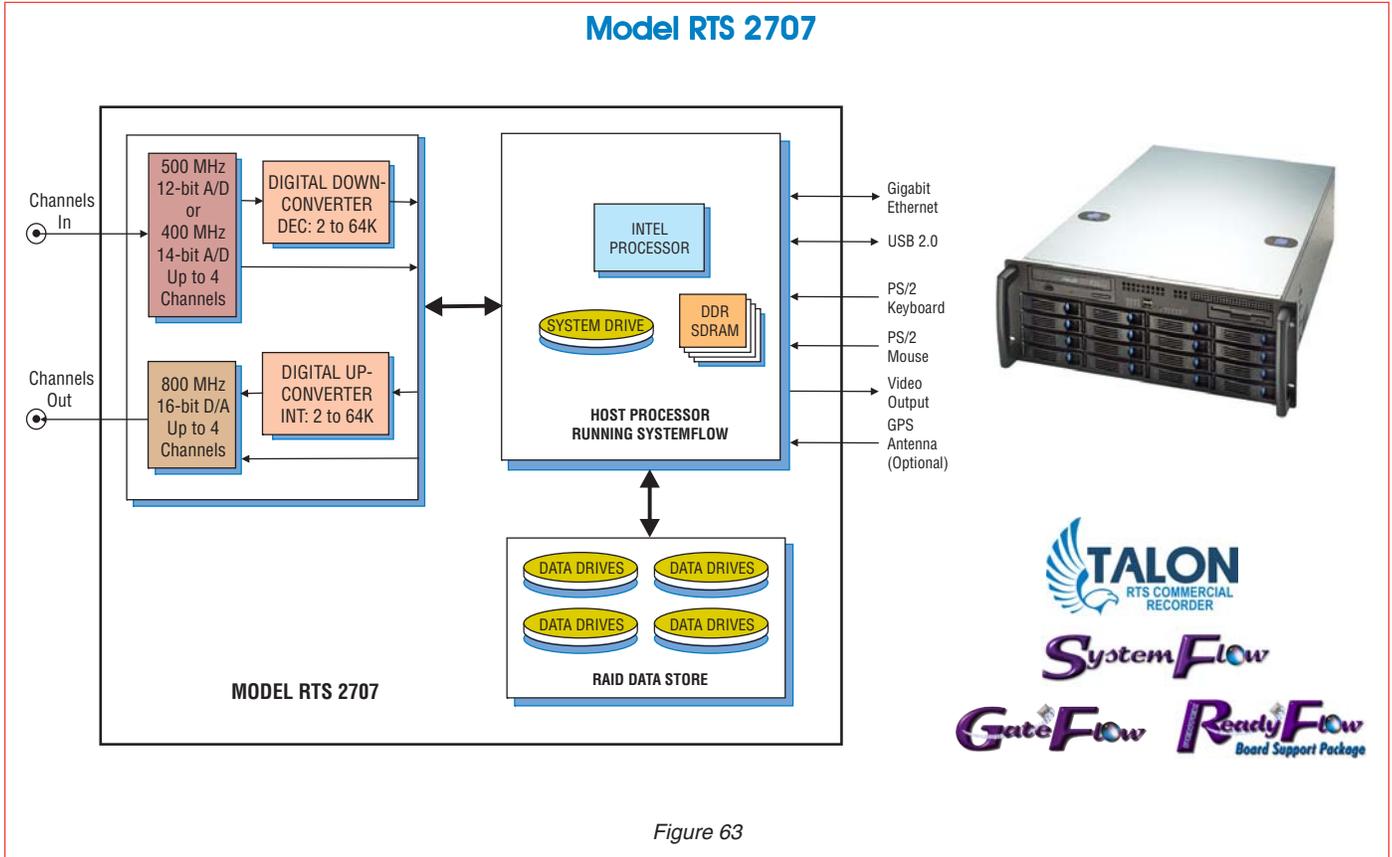
Figure 63

The Talon RTS 2707 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2707 uses 12-bit, 500 MHz A/D converters and provides sustained recording rates up to 1.6 GB/sec in two-channel configuration.

The RTS 2707 uses Pentek's high-powered Virtex-6-based Cobalt modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate and DUC interpolation are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals.

Optional GPS time and position stamping allows the user to record this critical signal information.

Included with the system is the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the recorder. SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTS 2707 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2707 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2707 is configured in a 4U 19" rackmountable chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to increase channel counts and aggregate data rates.

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Products

Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rackmount Recorder

Model RTS 2709
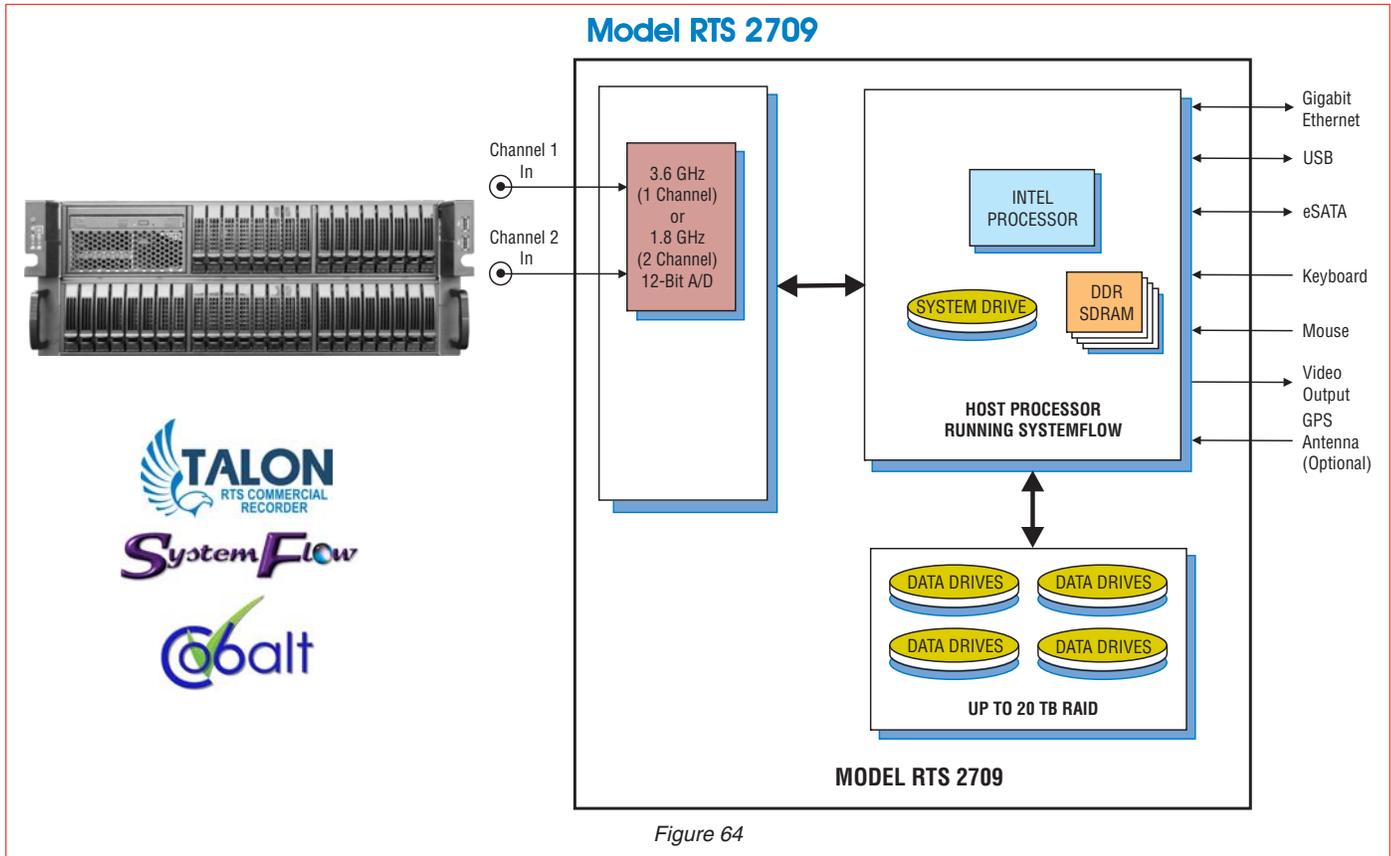
Figure 64

The Talon RTS 2709 is a turnkey system used for recording extremely high-bandwidth signals. The RTS 2709 uses a 12-bit, 3.6 GHz A/D converter and can provide sustained recording rates up to 3.2 GB/sec. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit wide consecutive samples, or as 16-bit wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word.)

The RTS 2709 uses Pentek's high-powered Virtex-6-based Cobalt boards that provide the data streaming engine for the high-speed A/D converter. Channel and packing modes as well as gate and trigger settings are among the GUI-selectable system parameters, providing complete control over this ultra wideband recording system.

Optional GPS time and position stamping allows the user to capture this information in the header of each data file.

The RTS 2709 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session.

Built on a Windows 7 Professional workstation, the RTS 2709 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2709 records data to the native NTFS file system that provides immediate access to the data. The RTS 2709 is configured in a 4U 19" rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

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Products

Two-Channel 10-Gigabit Ethernet Rackmount Recorder

Model RTS 2715
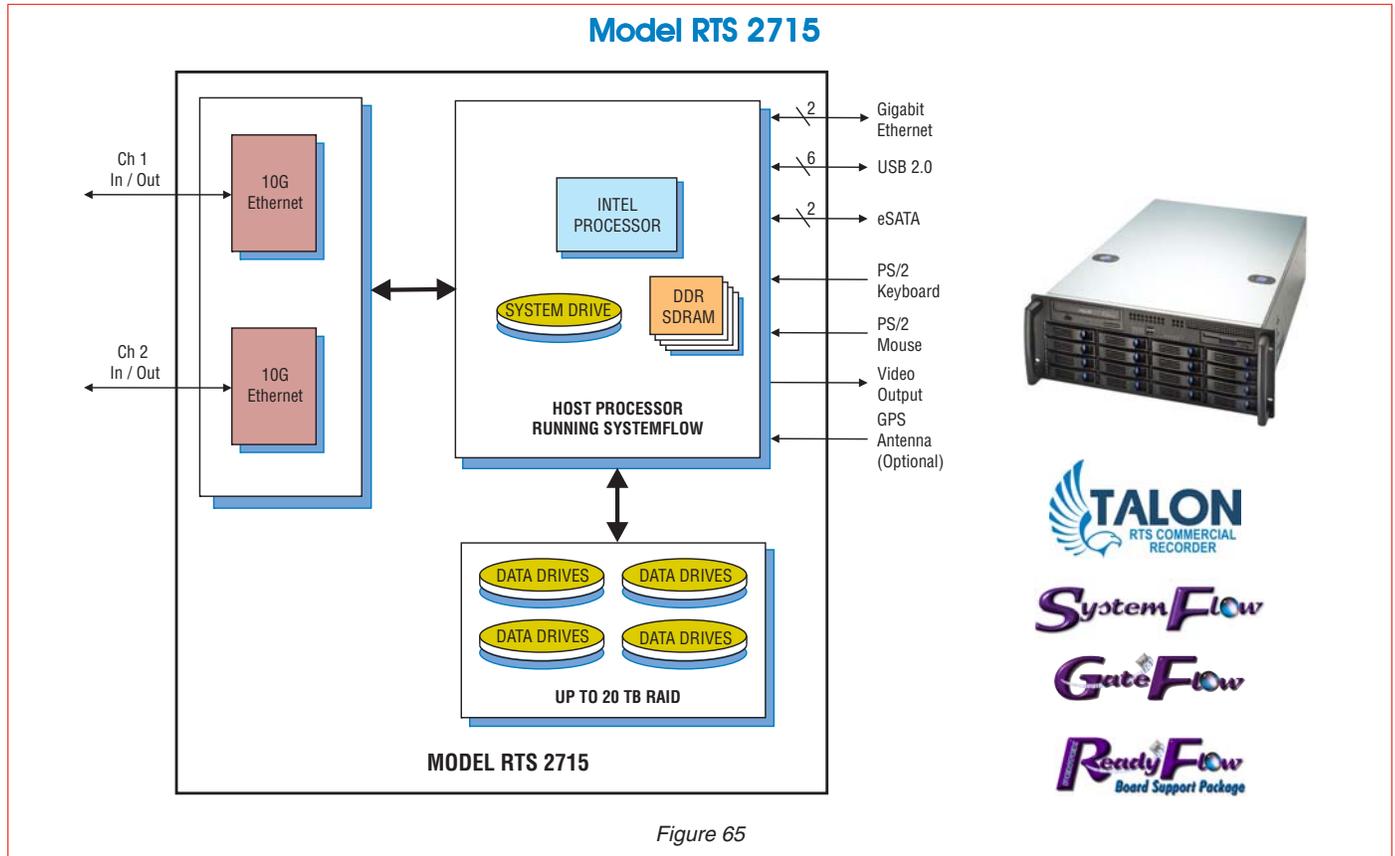
Figure 65

The Talon RTS 2715 is a complete turnkey recording system for storing one or two 10 gigabit Ethernet (10 GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 2.0 GB/sec.

Two rear panel SFP+LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces. Optional GPS time and position stamping accurately identifies each record in the file header.

The RTS 2715 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTS 2715 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2715 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2715 is configured in a 4U or 5U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

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PENTEK

Setting the Standard for Digital Signal Processing

Products

Eight-Channel Serial FPDP Rackmount Recorder

Model RTS 2716

Ch 1 In / Out — Serial FPDP
Ch 2 In / Out — Serial FPDP
Ch 3 In / Out — Serial FPDP
Ch 4 In / Out — Serial FPDP
Ch 5 In / Out — Serial FPDP
Ch 6 In / Out — Serial FPDP
Ch 7 In / Out — Serial FPDP
Ch 8 In / Out — Serial FPDP

INTEL PROCESSOR
SYSTEM DRIVE
DDR SDRAM
HOST PROCESSOR RUNNING SYSTEMFLOW

2 — Gigabit Ethernet
6 — USB 2.0
2 — eSATA
PS/2 Keyboard
PS/2 Mouse
Video Output
GPS Antenna (Optional)

DATA DRIVES DATA DRIVES
DATA DRIVES DATA DRIVES
UP TO 20 TB RAID

MODEL RTS 2716

TALON RTS COMMERCIAL RECORDER

SystemFlow

Figure 66

The Talon RTS 2716 is a complete turnkey recording system capable of recording and playing multiple serial FPDP data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.4 GB/sec.

The RTS 2716 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625,

2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 425 MB/sec per serial FPDP link.

Built on a server-class Windows 7 Professional workstation, the RTS 2716 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2716 records data to the native NTFS file system, providing immediate access to the data.

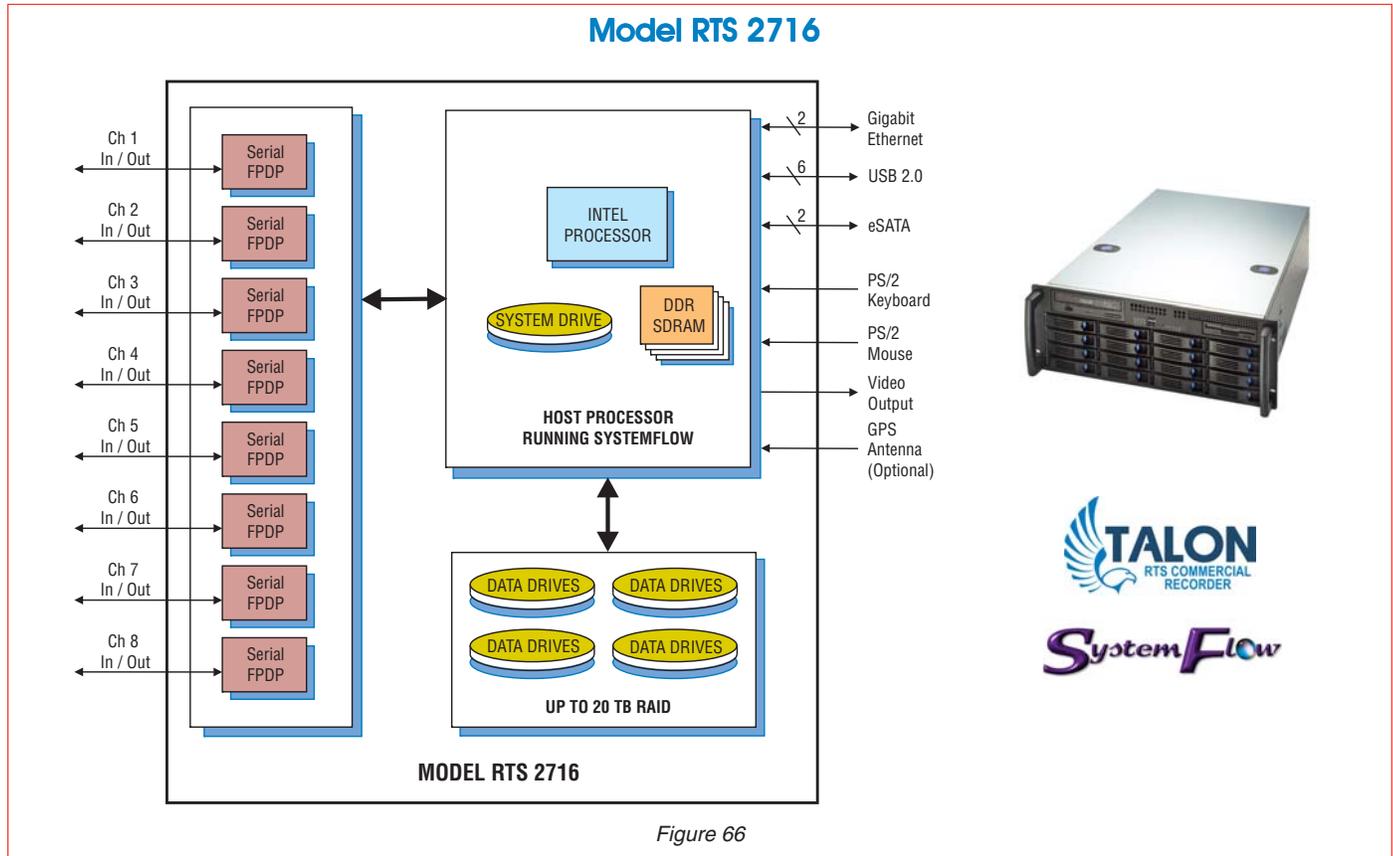The RTS 2716 is configured in a 4U or 5U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Up to 24 hot-swappable SATA drives are optionally available, allowing up to 20 terabytes of real-time data storage space in a single chassis.

The RTS 2716 includes the SystemFlow Recording Software, which features a Windows-based GUI that provides a simple and intuitive means to configure and control the system.

55

Products

Four-Channel RF/IF 200 MS/sec Rugged Portable Recorder

Model RTR 2726

Figure 67
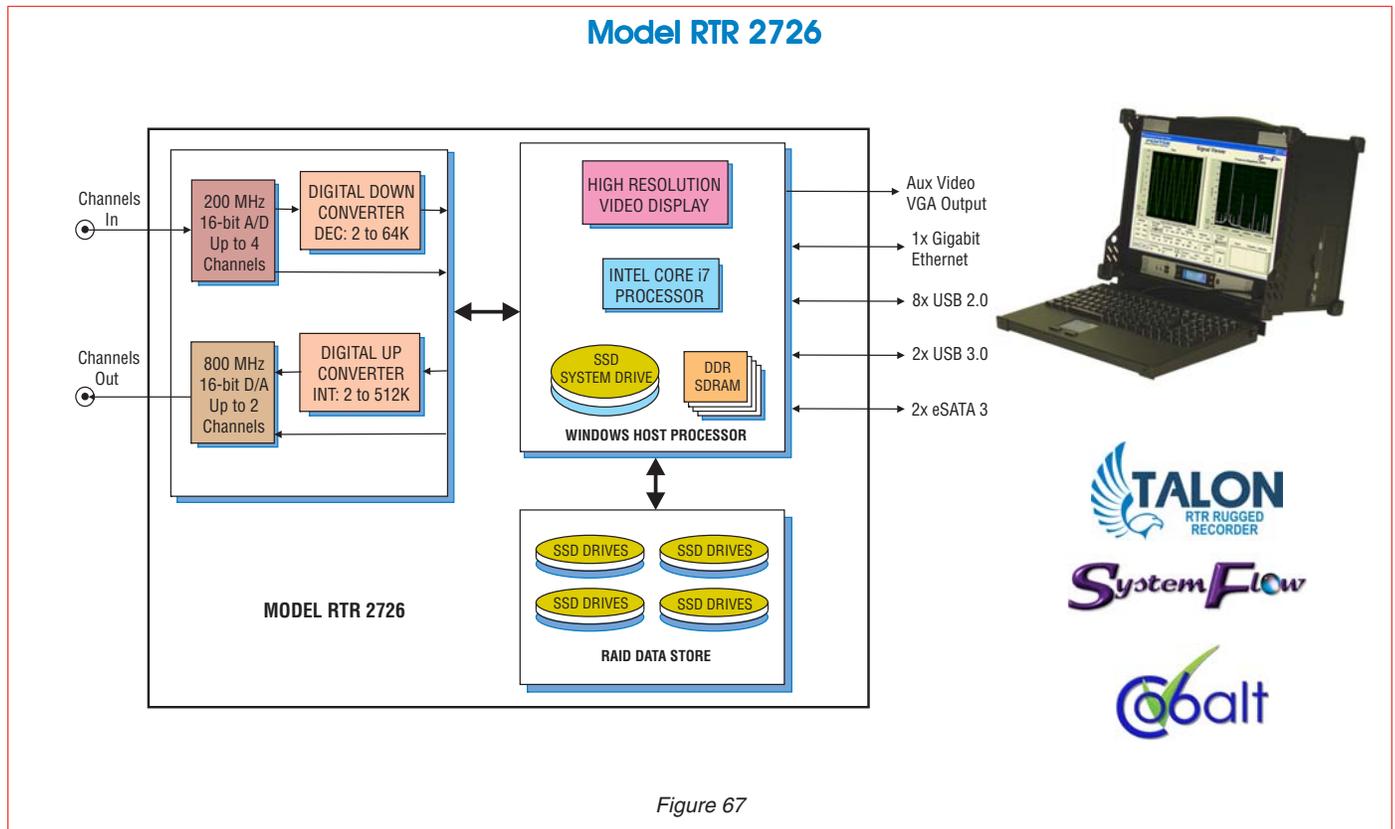
The Talon RTR 2726 is a turnkey, multiband recording and playback system designed to operate under conditions of shock and vibration. It allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2726 provides sustained recording rates of up to 1.6 GB/sec in a four-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2726 is supplied in a small footprint portable package measuring just 16.9" W x 9.5" D x 13.4" H and weighing about 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor, a high-resolution 17" LCD monitor, and a high-performance SATA RAID controller.

At the heart of the RTR 2726 are Pentek Cobalt Series Virtex-6 software radio boards featuring A/D and D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system. Optional GPS time and position stamping allows the user to record this critical signal information.

It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2726 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide a storage capacity of up to 3.8 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2726 performs well in ground, shipborne and airborne environments.

Products

Two-Channel RF/IF 500 MS/sec Rugged Portable Recorder

Model RTR 2727

Figure 68

The Talon RTR 2727 is a turnkey, multiband recording and playback system designed to operate under conditions of shock and vibration. It allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2727 provides sustained recording rates of up to 2.0 GB/sec in a two-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2727 is supplied in a small footprint portable package measuring just 16.9" W x 9.5" D x 13.4" H and weighing about 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor, a high-resolution 17" LCD monitor, and a high-performance SATA RAID controller.

At the heart of the RTR 2727 are Pentek Cobalt Series Virtex-6 software radio boards featuring A/D and D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system. Optional GPS time and position stamping allows the user to record this critical signal information.

It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2727 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide a storage capacity of up to 3.8 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2727 performs well in ground, shipborne and airborne environments.

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Products

Eight-Channel Serial FPDP Rugged Portable Recorder

Model RTR 2736
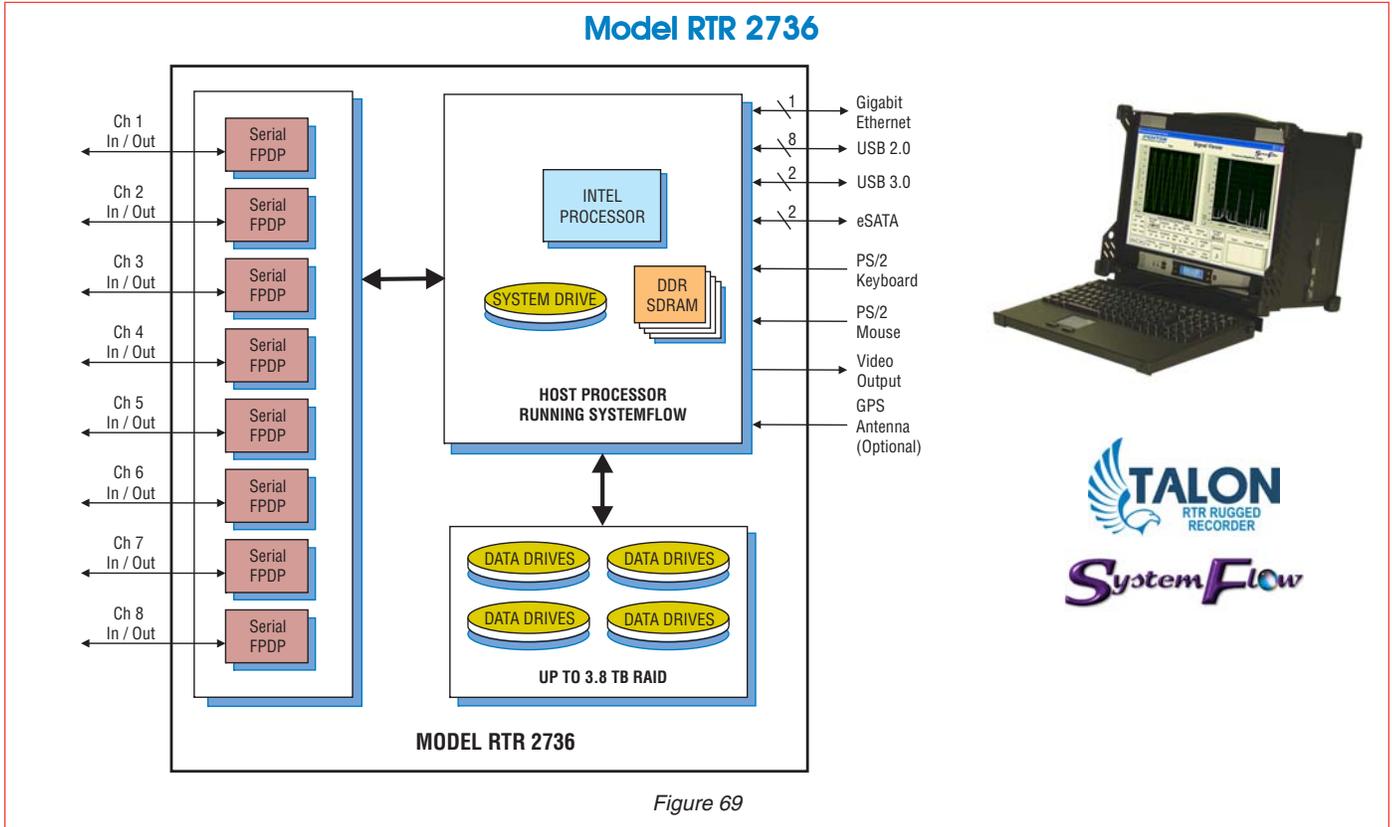
Figure 69

The Talon RTR 2736 is a complete turnkey recording system designed to operate under conditions of shock and vibration. It records and plays back multiple serial FPDP data streams in a rugged, lightweight portable package. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 1.6 GB/sec.

The RTR 2736 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 200 MB/sec per serial FPDP link.

The RTR 2736 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

The RTR 2736 is configured in a portable, lightweight chassis with eight hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2736 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide storage capacities of up to 3.8 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

Products

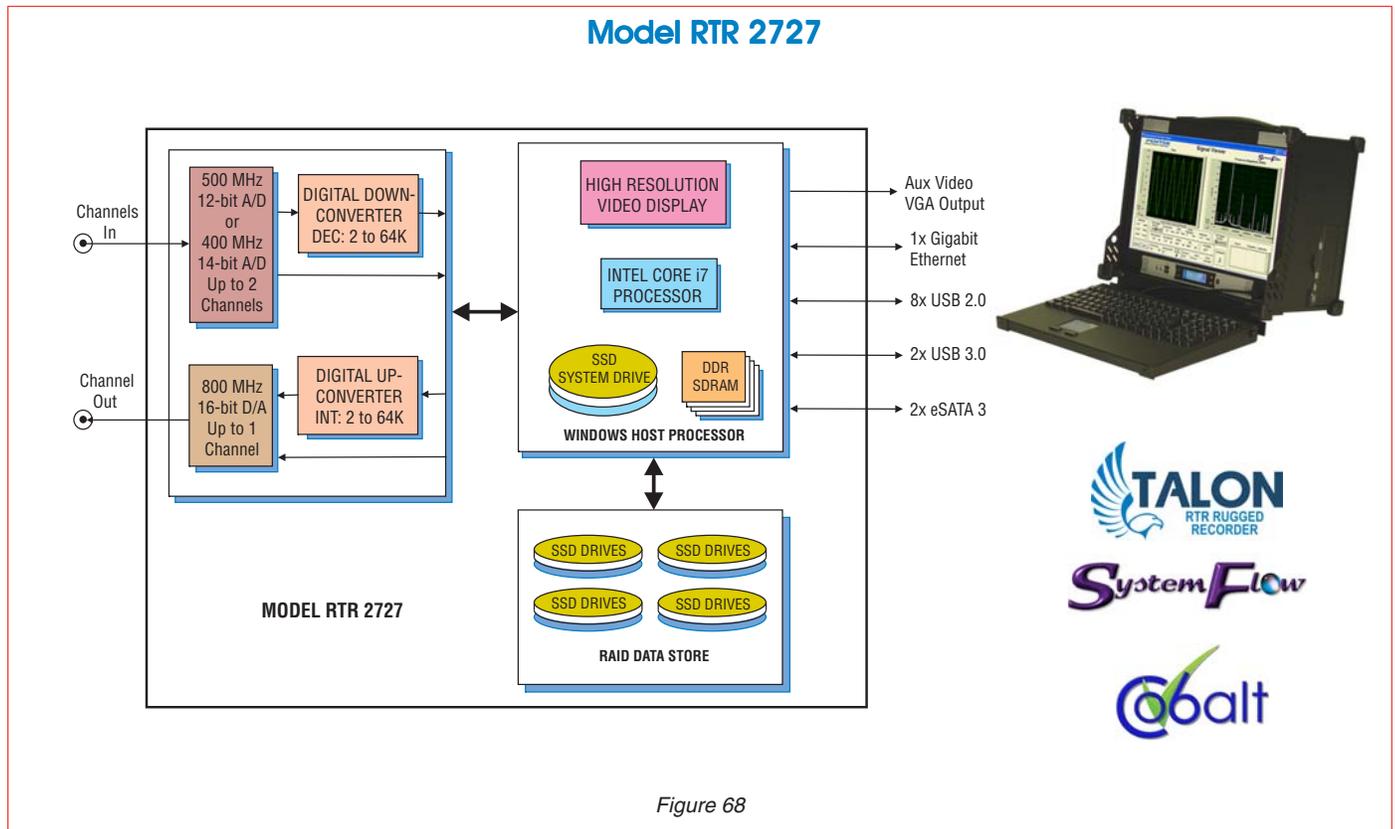## Eight-Channel RF/IF 200 MS/Sec Rugged Rackmount Recorder

Model RTR 2746

Figure 70
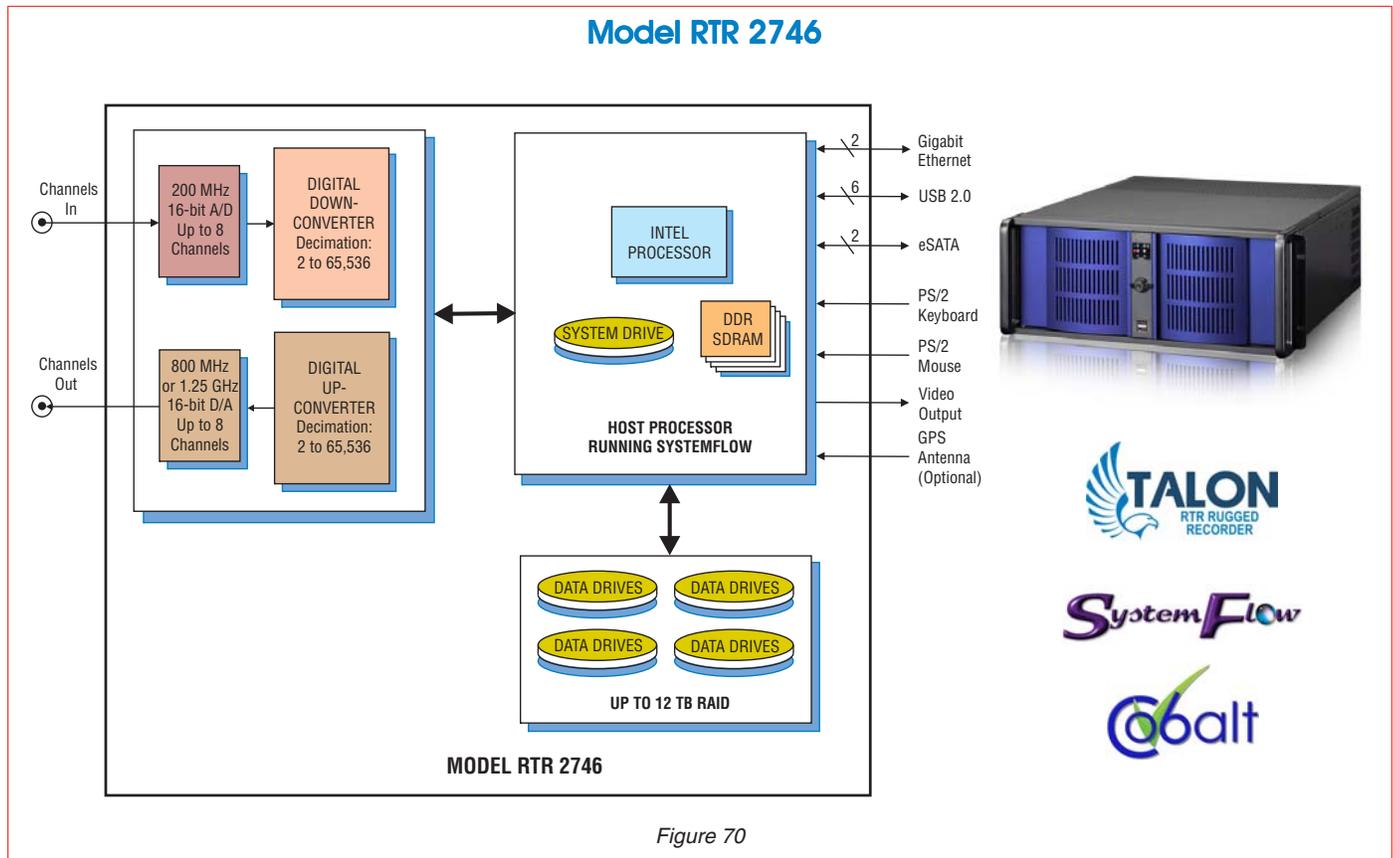
The Talon RTR 2746 is a turnkey multiband recording and playback system designed to operate under conditions of shock and vibration. The RTR 2746 is intended for military, airborne, and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (solid-state drive) storage, the RTR 2746 can be configured to stream data to and from disk at rates as high as 2.0 GB/sec.

The RTR 2746 uses Pentek's high-performance Virtex-6-based Cobalt boards, that provide flexibility in channel count with optional digital downconversion capabilities. Optional 16-bit, 800 MHz or 1.25 GHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate, and DUC interpolation are among the GUI-selectable system parameters, that provide a fully programmable system.

The 24 hot-swappable SSD's provide storage capacity of up to 12 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2746 performs well in ground, shipborne and airborne environments.

The RTR 2746 is configured in a 4U 19" rugged rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC. Multiple RAID levels, including 0, 1, 5, 6, 10, and 50, provide a choice for the required level of redundancy.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

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Products

Four-Channel RF/IF 500 MS/Sec Rugged Rackmount Recorder

Model RTR 2747
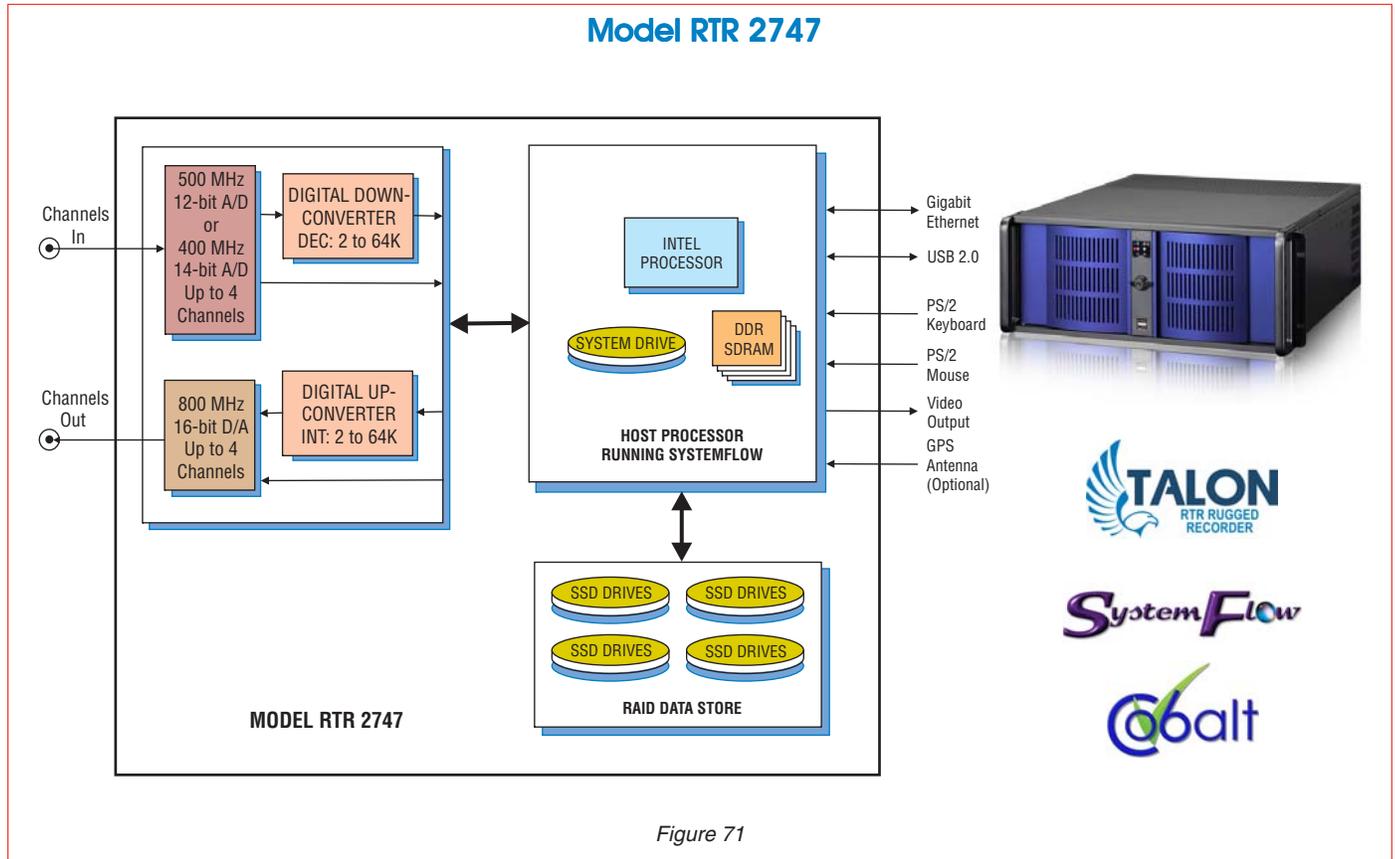
Figure 71

The Talon RTR 2747 is a turnkey multiband recording and playback system designed to operate under conditions of shock and vibration. The RTR 2747 is intended for military, airborne, and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (solid-state drive) storage, the RTR 2747 can be configured to stream data to and from disk at rates as high as 4.0 GB/sec.

The RTR 2747 uses Pentek's high-performance Virtex-6-based Cobalt boards, that provide flexibility in channel count with optional digital downconversion capabilities. Optional 16-bit, 800 MHz converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate, and DUC interpolation are among the GUI-selectable system parameters, that provide a fully programmable system.

The hot-swappable SSD's provide storage capacity of up to 11.5 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2747 performs well in ground, shipborne and airborne environments.

The RTR 2747 is configured in a 4U 19" rugged rackmountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC. Multiple RAID levels, including 0, 1, 5, 6, 10, and 50, provide a choice for the required level of redundancy.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

Products

Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rugged Rackmount Recorder

Model RTR 2749

Figure 72
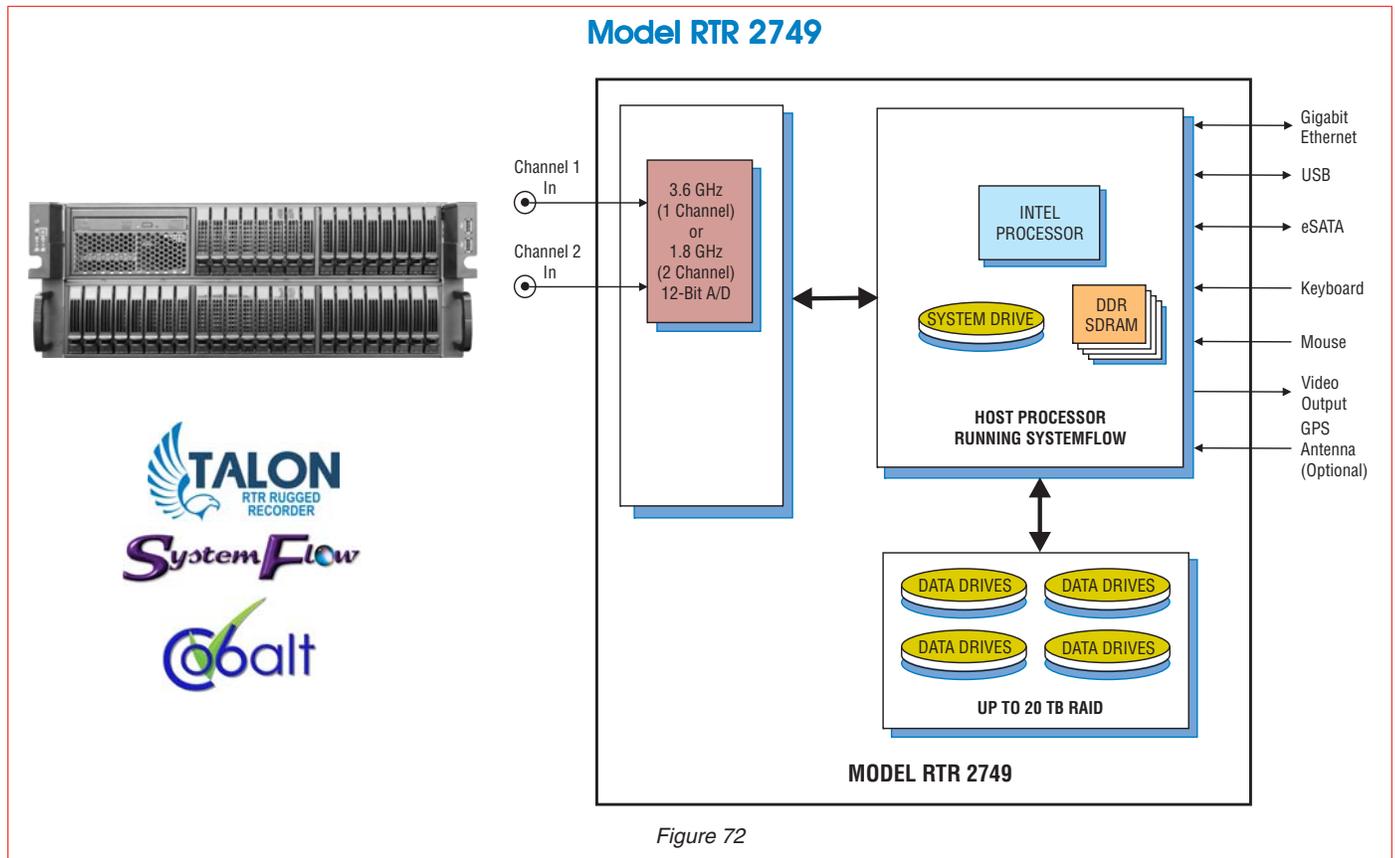
Designed to operate under conditions of shock and vibration, the Talon RTR 2749 is a turnkey system used for recording extremely high-bandwidth signals. The RTR 2749 uses a 12-bit, 3.6 GHz A/D converter and can provide sustained recording rates up to 3.2 GB/sec. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit wide consecutive samples, or as 16-bit wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word.)

The RTR 2749 uses Pentek's high-performance Virtex-6-based Cobalt boards that provide the data streaming engine for the high-speed A/D converter. Channel and packing modes as well as gate and trigger settings are among the GUI-selectable system parameters, providing complete control over this ultra-wideband recording system. Optional GPS time and position stamping allows the user to capture this information in the header of each data file.

The RTR 2749 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session.

Built on a Windows 7 Professional workstation, the RTR 2749 allows the user to install post-processing and analysis tools to operate on the recorded data. The hot-swappable SSDs provide a storage capacity of up to 19.2 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2749 performs well in ground, shipborne and airborne environments.

Products

Two-Channel 10-Gigabit Ethernet Rugged Rackmount Recorder

Model RTR 2755

Figure 73

Designed to operate under conditions of shock and vibration, the Talon RTR 2755 is a complete turnkey recording system for storing one or two 10 gigabit Ethernet (10 GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols.

Using highly-optimized solid-state drive storage technology, the system guarantees loss-free performance at aggregate recording rates up to 2.0 GB/sec.

Two rear panel SFP+ LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces.

Optional GPS time and position stamping accurately identifies each record in the file header.

The RTR 2755 includes the SystemFlow Recording Software that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2755 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2755 records data to the native NTFS file system, providing immediate access to the recorded data.

Because SSDs operate reliably under conditions of vibration and shock, the RTR 2755 performs well in ground, shipborne and airborne environments. The 24 hot-swappable SSD's provide a storage capacity of up to 12 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

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Products

Eight-Channel Serial FPDP Rugged Rackmount Recorder

Model RTR 2756

MODEL RTR 2756

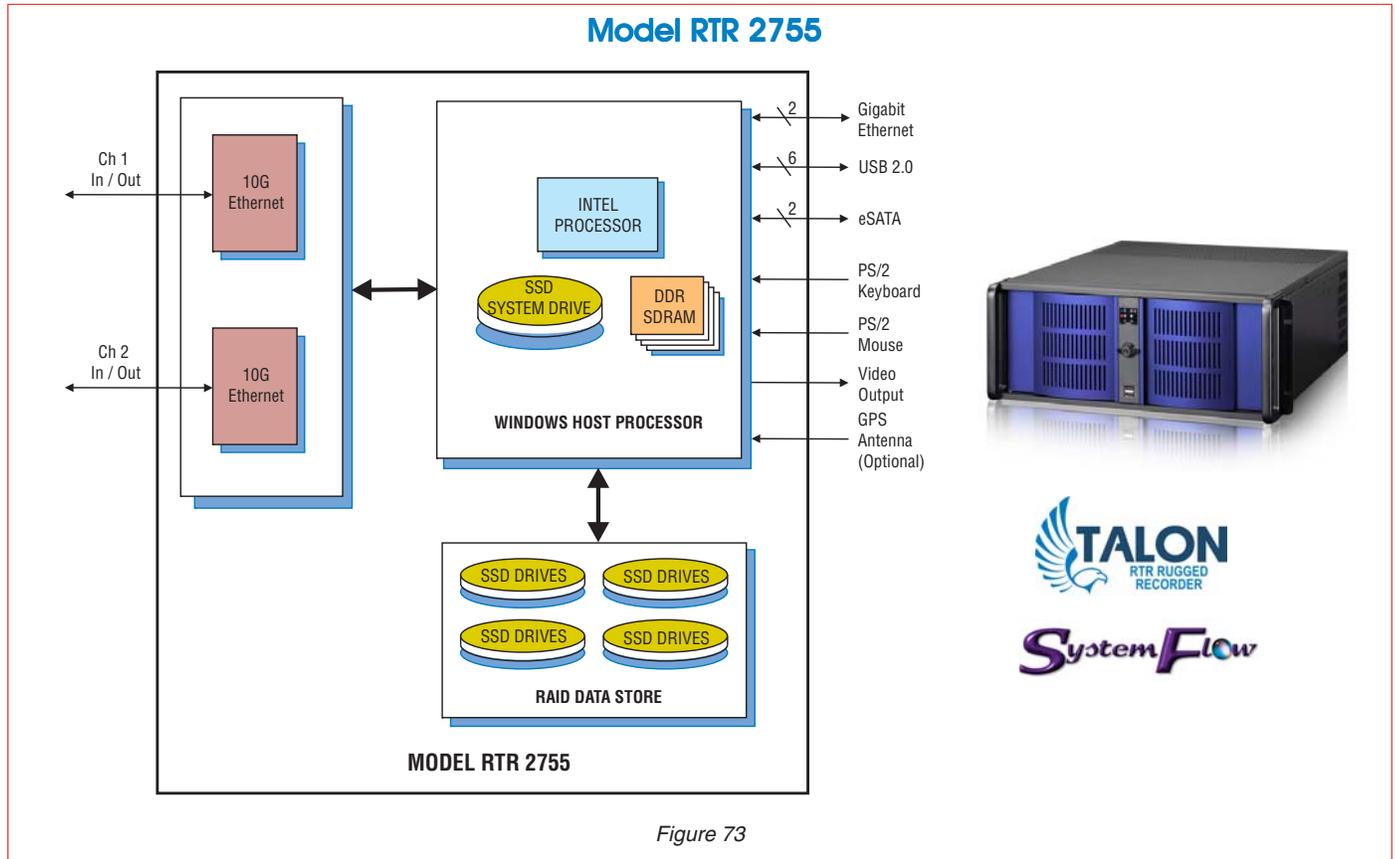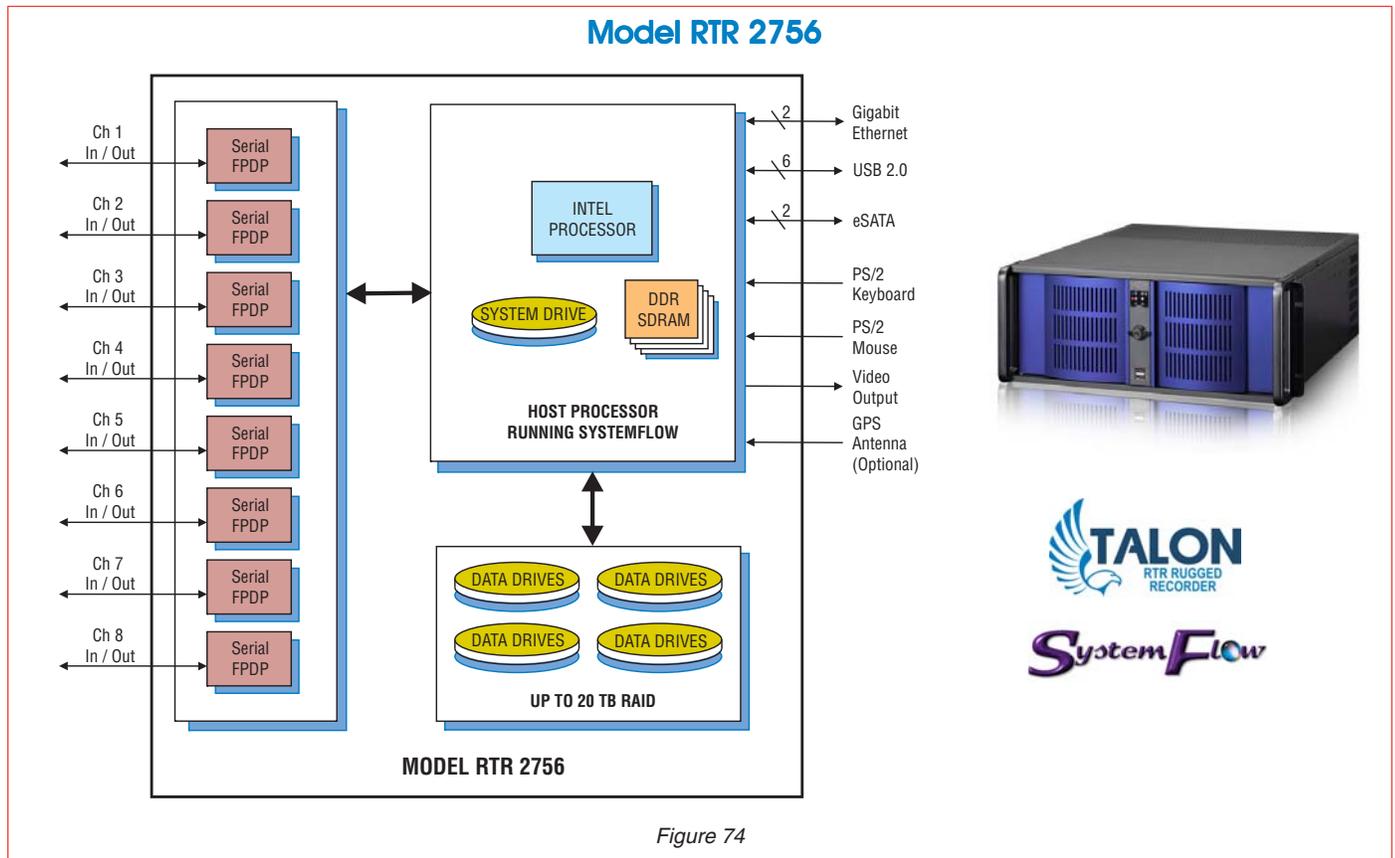*Figure 74*

Designed to operate under conditions of shock and vibration, the Talon RTR 2756 is a complete turnkey recording system capable of recording and playing multiple serial FPDP data streams. It is ideal for capturing any type of streaming sources and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.4 GB/sec.

The RTR 2756 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber to accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 425 MB/sec per serial FPDP link.

Built on a server-class Windows 7 Professional workstation, the RTR 2756 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2756 records data to the native NTFS file system, providing immediate access to the data.

Because SSDs operate reliably under conditions of vibration and shock, the RTR 2756 performs well in ground, ship and airborne environments. Configurable with as many as 40 hot-swappable SSDs, the RTR 2756 can provide storage capacities of up to 19.2 TB in a rugged 4U chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

Multiple RAID levels, including 0,1,5, 6, 10 and 50 provide a choice for the required level on redundancy. Redundant power supplies are optionally available to provide a robust and reliable high-performance recording system.

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Products

Four-Channel RF/IF 200 MS/Sec Extreme 3U VPX Recorder

Model RTX 2786

CH 1 In — 200 MHz 16-bit A/D — DIGITAL DOWN-CONVERTER

CH 2 In — 200 MHz 16-bit A/D — DIGITAL DOWN-CONVERTER

CH 3 In — 200 MHz 16-bit A/D — DIGITAL DOWN-CONVERTER

Out — 800 MHz 16-bit D/A — DIGITAL UPCONVERTER

Sample Clk / Reference In — CLOCK & SYNC GENERATOR — PROGRAM VCXO

INTEL PROCESSOR — SYSTEM DRIVE — DDR SDRAM — HOST PROCESSOR

2 Gigabit Ethernet
4 USB 2.0
Video Output

DATA DRIVES — RAID

MODEL 53621

MODEL RTX 2786
Three Record Channels and One Playback Channel.

TALON RTX EXTREME RECORDER

SystemFlow

Figure 75

The Talon RTX 2786 is a turnkey, RF/IF signal recorder designed to operate under extreme environmental conditions. Housed in a ½ ATR chassis, the RTX 2786 leverages Pentek's 3U VPX SDR modules to provide a rugged recording system with up to four 16-bit, 200 MHz A/D converters with built-in digital downconversion capabilities. Optionally, the RTX 2786 provides one 800 MHz, 16-bit D/A converter with a digital upconverter for signal playback or waveform generation. As shown in the block diagram, the maximum number of record channels with this option is three.

The RTX 2786 uses conduction cooling to draw heat from the system components allowing it to operate in reduced air environments. It includes 1.92 TB of solid-state data storage, that allows it to operate with no degradation under conditions of extreme shock and vibration. The system is hermetically sealed and provides five D38999 connectors for power and I/O with four SMA connectors for analog I/O.

The RTX 2786 includes Pentek's SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

The user API allows users to integrate the recorder as a subsystem of a larger system. The API is provided as a C-callable library and allows for the recorder to be controlled over Ethernet, thus providing the ability to remotely control the recorder from a custom interface.

Four built-in solid-state drives provide reliable, high-speed storage with a total capacity of 1.92 TB.

Products

Pentek SystemFlow Recording Software for Analog Recorders

Recorder Interface

Hardware Configuration Interface

Signal Viewer
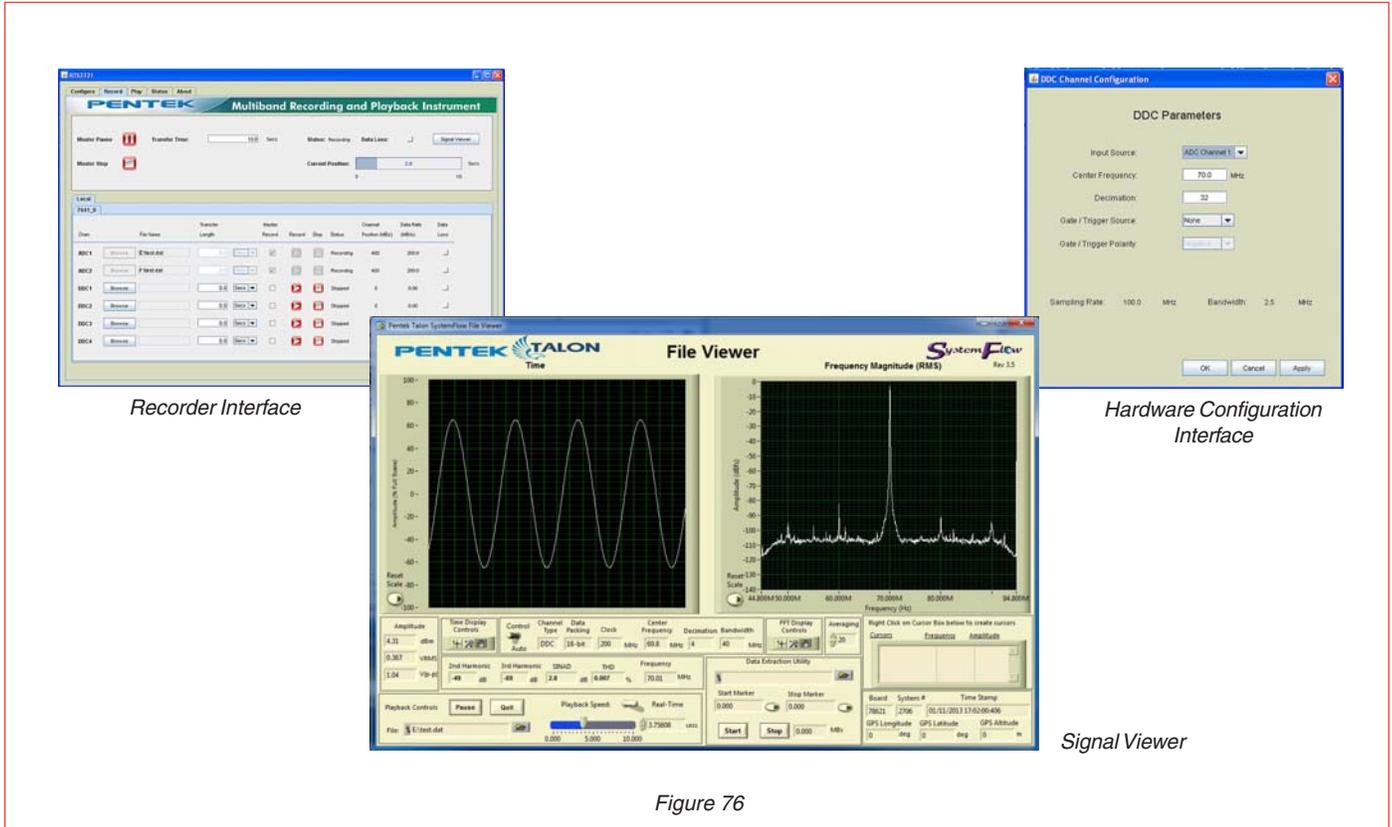
Figure 76

The Pentek SystemFlow Recording Software for Analog Recorders provides a rich set of function libraries and tools for controlling all Pentek high-speed real-time recording systems. SystemFlow software allows developers to configure and customize system interfaces and behavior.

The **Recorder Interface** includes configuration, record, playback and status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperatures and voltage levels.

The **Hardware Configuration Interface** provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The SystemFlow **Signal Viewer** includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

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Products

Pentek SystemFlow Recording Software for Digital Recorders

Configure Screen

Hardware Configuration

Recording and Playback Screen
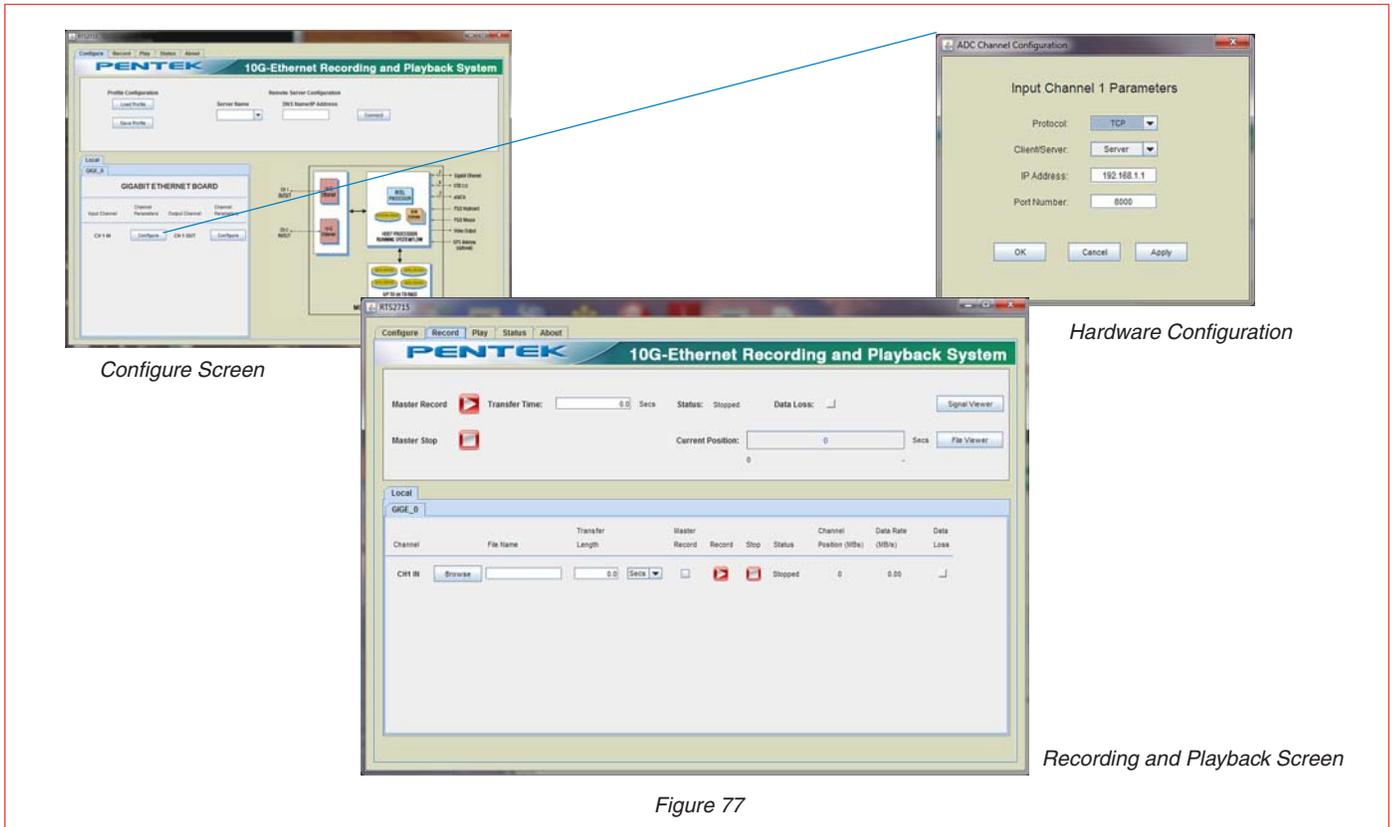
Figure 77

The SystemFlow Software for Digital Resorders provides the user with a control interface for the recording system. It includes Configuration, Record, Playback, and Status screens, each with intuitive controls and indicators.

The user can easily move between screens to set configuration parameters, control and monitor a recording, and play back a recorded stream. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The **Configure Screen** shows a block diagram of the system, and presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number.

The **Recording and Playback Screen** allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk-full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.

Applications

64-Channel Software Radio Recording System

Figure 78

Shown above is a 64-channel recording system utilizing two Pentek Cobalt 78662 PCIe boards. The 78662 samples four input channels at up to 200 megasamples per second, thereby accommodating input signals with up to 80 MHz bandwidth.

Factory-installed in the FPGA of each 78662 is a powerful DDC IP core containing 32 channels. Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within each bank share a commo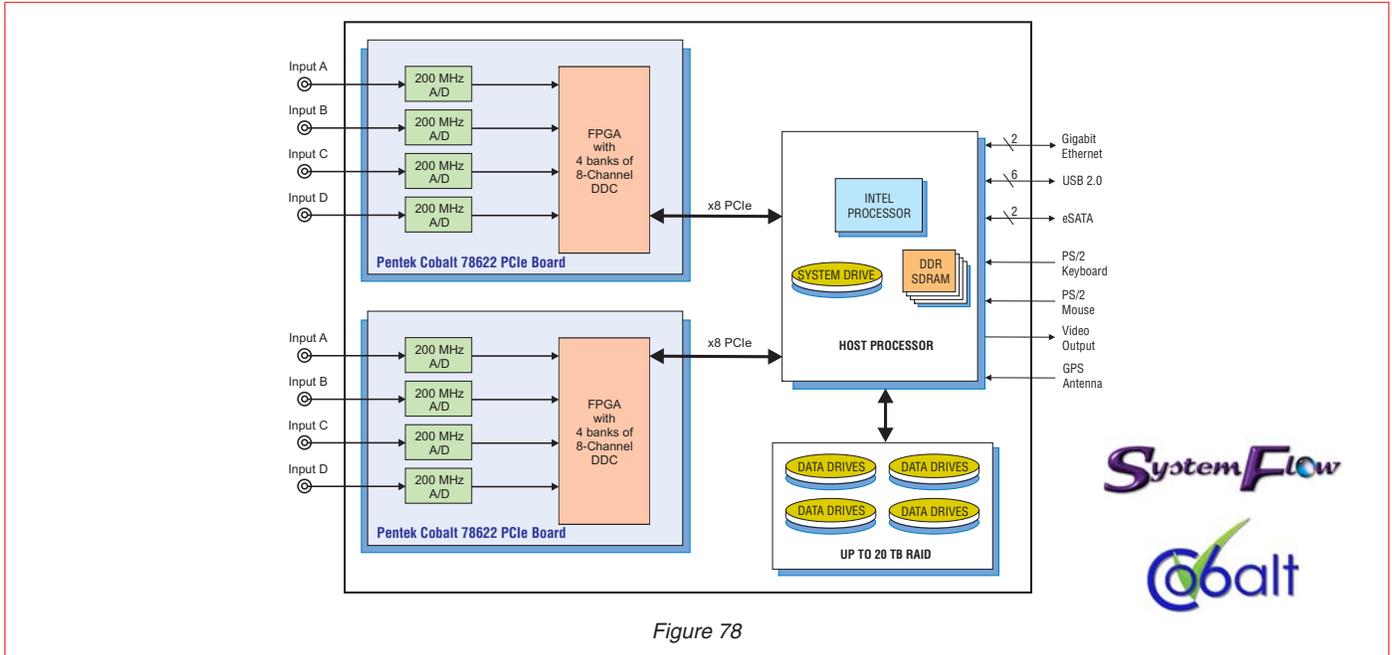n decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

An internal timing bus provides all timing and synchronization required by the eight A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

Built on a Windows 7 Professional workstation with high performance Intel® Core™ i7 processor this system allows the user to install post processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data.

Included with this system is Pentek's SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.

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Applications

L-Band Signal Processing System
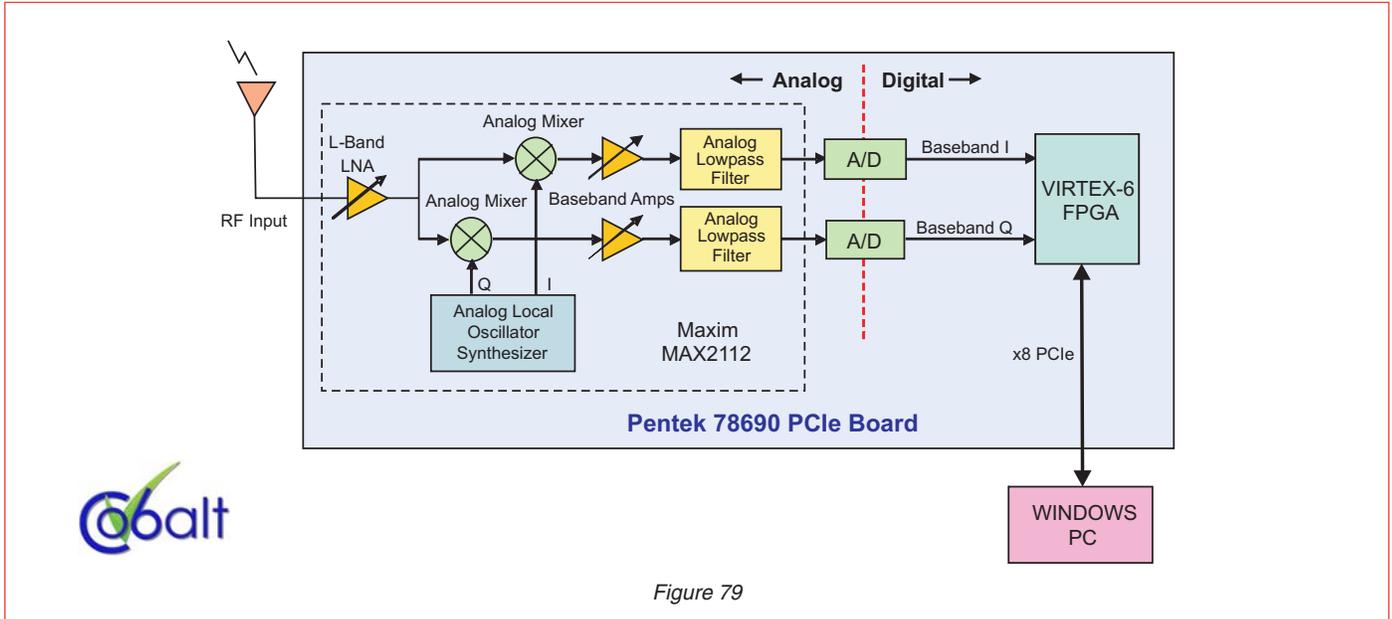
Figure 79

The Cobalt Model 78690 L-Band RF Tuner targets reception and processing of digitally-modulated RF signals such as satellite television and terrestrial wireless communications. The 78690 requires only an antenna and a host computer to form a complete L-band SDR development platform.

This system receives L-Band signals between 925 MHz and 2175 MHz directly from an antenna. Signals above this range such as C Band, Ku Band and K band can be downconverted to L-Band through an LNB (Low Noise Block) downconverter installed in the receiving antenna.

The Maxim Max2112 L-Band Tuner IC features a low-noise amplifier with programmable gain from 0 to 65 dB and a synthesized local oscillator programmable from 925 to 2175 MHz. The complex analog mixer translates the input signals down to DC. Baseband amplifiers provide programmable gain from 0 to 15 dB in steps of 1 dB. The bandwidth of the baseband lowpass filters can be programmed from 4 to 40 MHz . The Maxim IC accommodates full-scale input levels of -50 dBm to +10 dbm and delivers I and Q complex baseband outputs.

The complex I and Q outputs are digitized by two 200 MHz 16-bit A/D converters operating synchronously.

The Virtex-6 FPGA is a powerful resource for recovering and processing a wide range of signals while supporting decryption, decoding, demodulation, detection, and analysis. It is ideal for intercepting or monitoring traffic in SIGINT and COMINT applications. Other applications that benefit include mobile phones, GPS, satellite terminals, military telemetry, digital video and audio in TV broadcasting satellites, and voice, video and data communications.

This L-Band signal processing system is ideal as a front end for government and military systems. Its small size adderesses space-limited applications. Ruggedized options are also available from Pentek with the Models 71690 XMC module and the 53690 OpenVPX board to address UAV applications and other severe environments.

Development support for this system is provided by the Pentek ReadyFlow board support package for Windows, Linux and VxWorks. Also available is the Pentek GateFlow FPGA Design Kit to support custom algorithm development.

Applications

8-Channel OpenVPX Beamforming System
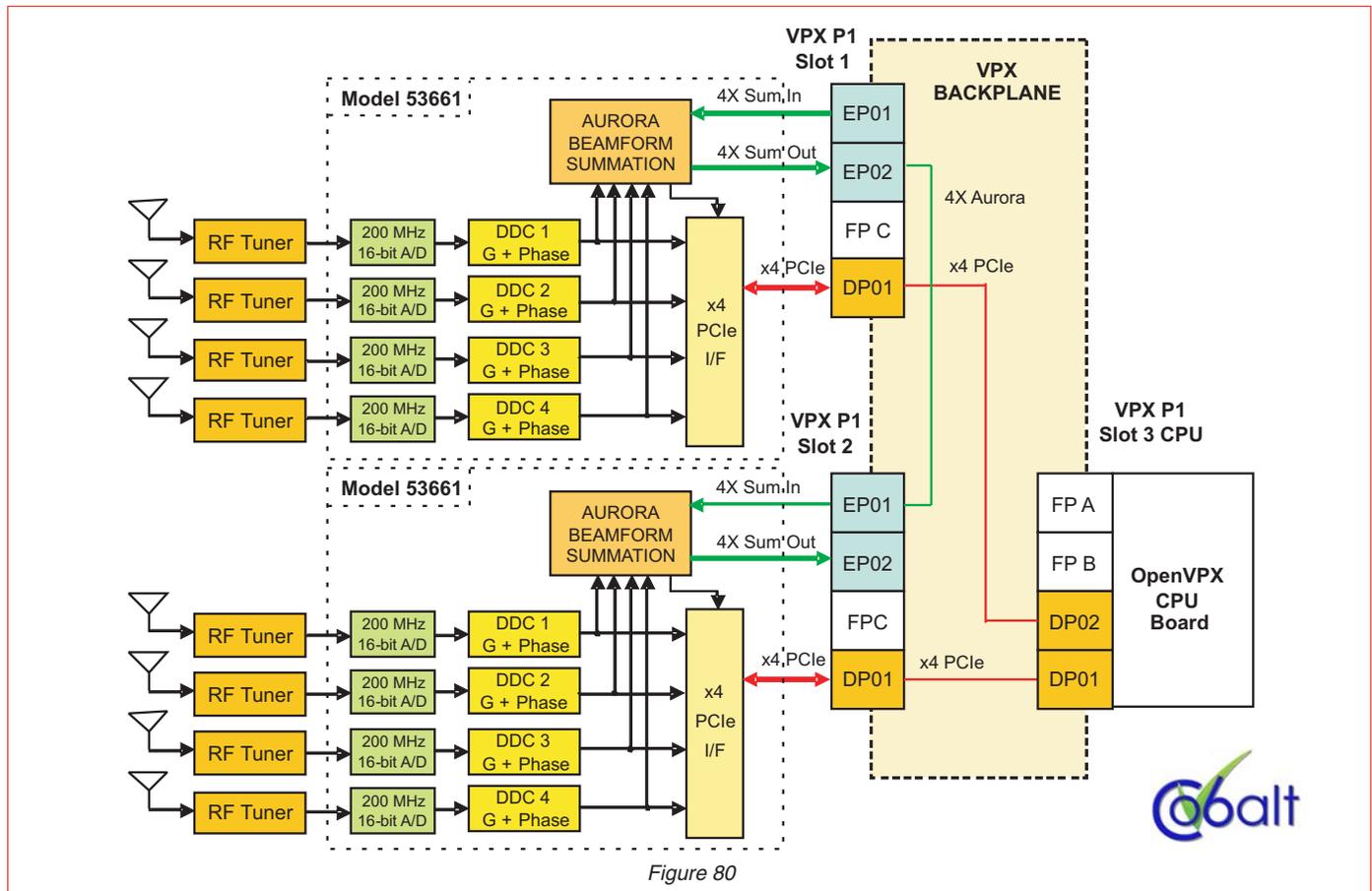
Figure 80

Two Model 53661 boards are installed in slots 1 and 2 of an OpenVPX backplane, along with a CPU board in slot 3. Eight dipole antennas designed for receiving 2.5 GHz signals feed RF Tuners containing low noise amplifiers, local oscillators and mixers. The RF Tuners translate the 2.5 GHz antenna frequency signal down to an IF frequency of 50 MHz.

The 200 MHz 16-bit A/Ds digitize the IF signals and perform further frequency downconversion to baseband, with a DDC decimation of 128. This provides I+Q complex output samples with a bandwidth of about 1.25 MHz. Phase and gain coefficients for each channel are applied to steer the array for directionality.

The CPU board in VPX slot 3 sends commands and coefficients across the backplane over two x4 PCIe links, or OpenVPX "fat pipes".

The first four signal channels are processed in the upper left 53661 board in VPX slot 1, where the 4-channel beamformed sum is propagated through the 4X Aurora Sum Out link across the backplane to the 4X Aurora Sum In port on the second 53661 in slot 2. The 4-channel local summation from the second 53661 is added to the propagated sum from the first board to form the complete 8-channel sum. This final sum is sent across the x4 PCIe link to the CPU card in slot 3.

Assignment of the three OpenVPX 4X links on the Model 53661 boards is simplified through the use of a crossbar switch which allows the 53661 to operate with a wide variety of different backplanes.

Because OpenVPX does not restrict the use of serial protocols across the backplane links, mixed protocol architectures like the one shown are fully supported. ➤

Applications

8-Channel OpenVPX Beamforming Demo system

Beamforming Demo Control Panel   Theoretical 7-lobe Beamforming Patern   Real-Life Beamforming Patern

Figure 81
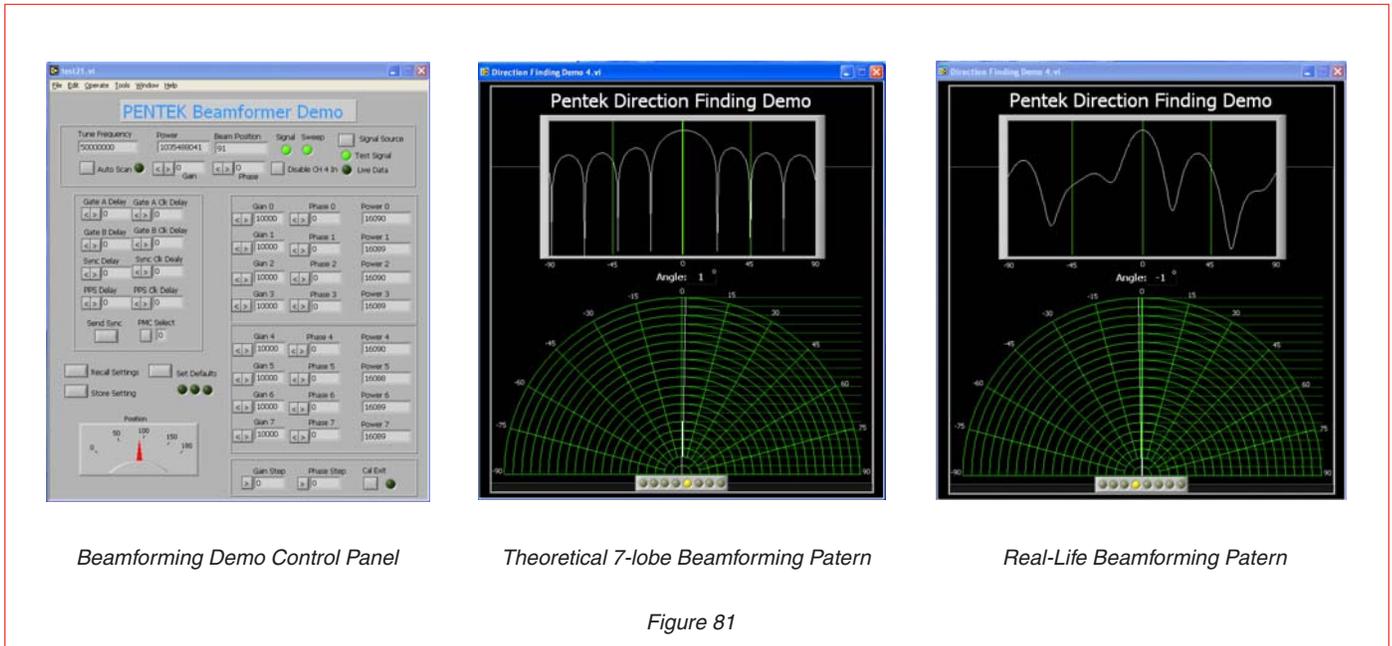
▶ Beamforming Demo System

The beamforming demo system is equipped with a Control Panel that runs under Windows on the CPU board. It includes an automatic signal scanner to detect the strongest signal frequency arriving from a test transmitter. This frequency is centered around the 50 MHz IF frequency of the RF downconverter. Once the frequency is identified, the eight DDCs are set accordingly to bring that signal down to 0 Hz for summation.

The control panel software also allows specific hardware settings for all of the parameters for the eight channels including gain, phase, and sync delay.

An additional display shows the beam-formed pattern of the array. This display is formed by adjusting the phase shift of each of the eight channels to provide maximum sensitivity across arrival angles from -90° to +90° perpendicular to the plane of the array.

The classic 7-lobe pattern for an ideal 8-element array for a signal arriving at 0° angle (directly in front of the array) is shown above. Below the lobe pattern is a polar plot showing a single vector pointing to the computed angle of arrival. This is derived from identifying the lobe with the maximum response.

An actual plot of a real-life transmitter is also shown for a source directly in front of the display. In this case the perfect lobe pattern is affected by physical objects, reflections, cable length variations and minor differences in the antennas. Nevertheless, the directional information is computed quite well. As the signal source is moved left and right in front of the array, the peak lobe moves with it, changing the computed angle of arrival.

This demo system is available online at Pentek. If you are interested in viewing a live demonstration, please let us know of your interest by clicking on this link:
Beamforming Demo.

Links

The following links provide you with additional information about the Pentek products presented in this handbook: just click on the model number. Links are also provided to other handbooks or catalogs that may be of interest in your software radio development projects.

Model	Description	Page
7142	Multichannel Transceiver with Virtex-4 FPGAs - PMC/XMC	19
7242	Multichannel Transceiver with Virtex-4 FPGAs - 6U cPCI	19
7342	Multichannel Transceiver with Virtex-4 FPGAs - 3U cPCI	19
7642	Multichannel Transceiver with Virtex-4 FPGAs - PCI	19
7742	Multichannel Transceiver with Virtex-4 FPGAs - Full-length PCIe	19
7842	Multichannel Transceiver with Virtex-4 FPGAs - Half-length PCIe	19
5342	Multichannel Transceiver with Virtex-4 FPGAs - 3U VPX	19
7142-428	Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter - PMC/XMC	20
7242-428	Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter- 6U cPCI	20
7342-428	Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter- 3U cPCI	20
7642-428	Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter- PCI	20
7742-428	Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter- Full-length PCIe	20
7842-428	Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter- Half-length PCIe	20
5342-428	Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter- 3U VPX	20
7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PMC/XMC	21
7250	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 6U cPCI	21
7350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U cPCI	21
7650	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - PCI	21
7750	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Full-length PCIe	21
7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - Half-length PCIe	21
5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX	21
7151	256-Channel DDC with Quad 200 MHz, 16-bit A/D - PMC	22
7251	256-Channel DDC with Quad 200 MHz, 16-bit A/D - 6U cPCI	22
7351	256-Channel DDC with Quad 200 MHz, 16-bit A/D - 3U cPCI	22
7651	256-Channel DDC with Quad 200 MHz, 16-bit A/D - PCI	22
7751	256-Channel DDC with Quad 200 MHz, 16-bit A/D - Full-length PCIe	22
7851	256-Channel DDC with Quad 200 MHz, 16-bit A/D - Half-length PCIe	22
5351	256-Channel DDC with Quad 200 MHz, 16-bit A/D - 3U VPX	22
7152	32-Channel DDC with Quad 200 MHz, 16-bit A/D - PMC	23
7252	32-Channel DDC with Quad 200 MHz, 16-bit A/D - 6U cPCI	23
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